

ESD full chip simulation: HBM and CDM requirements and simulation approach

E. Franell¹, S. Druen², H. Gossner², and D. Schmitt-Landsiedel¹

¹Institute for Technical Electronics, Technical University Munich, Germany

²Infineon Technologies AG, Munich, Germany

Abstract. Verification of ESD safety on full chip level is a major challenge for IC design. Especially phenomena with their origin in the overall product setup are posing a hurdle on the way to ESD safe products. For stress according to the Charged Device Model (CDM), a stumbling stone for a simulation based analysis is the complex current distribution among a huge number of internal nodes leading to hardly predictable voltage drops inside the circuits.

This paper describes an methodology for Human Body Model (HBM) simulations with an improved ESD-failure coverage and a novel methodology to replace capacitive nodes within a resistive network by current sources for CDM simulation. This enables a highly efficient DC simulation clearly marking CDM relevant design weaknesses allowing for application of this software both during product development and for product verification.

1 Introduction

Robustness of ICs against electrostatic discharge (ESD) is one of the leading topics in actual chip design flows due to the shrinking of devices and especially gate oxide thicknesses in modern CMOS processes. ESD on chip level results in current discharge pulses (1A–10A) through a not mounted IC.

ESD protection conducts the discharge current through the chip on a safe path. Provided that the discharge path itself is safe, remaining possible failure sites may be found inside the core in elements which are not close to the discharge current path. Voltage differences on cells which are connected to more than one voltage domain are prone to cause this kind of problems.

The design optimization for HBM and especially CDM safety is still an evolutionary approach involving failure analysis and re-designs. This is expensive and may delay time-to-market of a product tremendously. Thus software based verification is required which predicts weaknesses of the IC design before tape-out.

Device simulation has established as powerful tool during the development of ESD protection concepts (Esmark, 2000), but due to the high numerical effort, it can only be applied for analysis of small structures, e.g. protection devices or parasitic structures. Some further efforts have been done searching for possible current paths through the IC (Liu, 2006). Furthermore, a layout-based verification of ESD-rules has been proposed (Zhan, 2005).

This paper will present ESD simulation methodologies for the verification of ULSI microchips, different from all established variants of ESD-simulation. The second section shows the requirements for a verification-oriented ESD simulation. Section 3 presents the simulation approach and a way to comply with the shown requirements. In Sect. 4 the functionality of the tool and the requirements for such software are demonstrated with a product example. The extension of this approach to CDM verification is discussed in Sect. 5. A conclusion is given in Sect. 6.

2 Full chip ESD-simulation – requirements

For ESD issues a complex netlist from circuit design contains too much information about non-relevant parts of the IC. Therefore the basic steps for an efficient ESD simulation are the reduction of complexity to an amount which allows a huge number of stress combinations for highly complex ICs. As it has been shown for a HBM type, 2 pin discharge with externally forced current a DC simulation of simplified netlists together with special simulation models is sufficient



Correspondence to: E. Franell
(enrico.franell@tum.de)

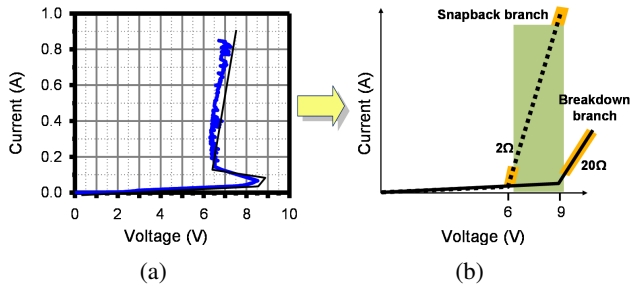


Fig. 1. Measured IV-curve and simplified model for ESD-protection elements with snapback behavior.

to detect design weaknesses in the ESD-protection (Druen, 2007).

Waveforms and failures could be reproduced in transient ESD simulations, but failure prediction was not satisfying (Etherton, 2006). A truly predictive and useful simulation approach needs to be based on the (huge) input database of a design project without major manual modification. Our approach to facilitate the verification is that a highly accurate transient simulation is typically not required.

2.1 Requirements

The demand for a predictive simulation in the product concept phase implicates that the ESD netlist can not be based on extraction from complete schematics and layouts. A second request is the product ESD-review for the final check of all ESD-rules. At this moment the final database for the product already exists and often achieves a complexity which makes manual checking very time consuming.

The device behaviour during an ESD pulse differs from normal operation conditions. At typical ESD current levels of several 100mA to several amperes MOS and bipolar devices typically expose snapback behaviour that must be handled by the ESD simulation. An example for a typical snapback IV characteristic is given in Fig. 1.

The characteristics of a snapback are the trigger voltage, here $V_{t1}=9$ V, and the snapback voltage $V_{SP}=6$ V. In the green zone, both characteristics may be valid depending on history. The yellow zones represents the invalid parts of the pwl descriptions.

2.2 Simulation concept

Our particular ESD netlist building and simulation process is based on the following five considerations:

1. In most cases a new design will employ a precharacterized I/O cell library. The ESD view has to provide all major ESD current paths through the I/O cell. Therefore, a much simplified ESD view for the library cells will be sufficient for chip level ESD simulation.

2. The setup of a proper ESD protection concept avoids destructive current paths through the IO cell logic or the chip core. Correspondingly simulation will still be correct when these blocks are excluded from the ESD netlist. An extremely simplified but sufficiently accurate ESD netlist can be built by plugging together the ESD views of the individual I/O cells in the pad ring to a pad ring netlist, adding the chip core supply mesh, the bondout, and merging it with the package netlist.
3. One of the main sources of ESD failures is the division of the IC into a certain number of electrical supply voltage domains or ground nets on one chip. This division requires additional protection elements and package concepts, which must be included in the simulation netlist.
4. The actual ESD standards provide opportunities to decrease the amount of stress combinations by exploiting the particular chip topology (EOS/ESD Association, 2001). The proposed simulation tool is able to build a stress plan which contains every relevant pin combination to yield full test coverage and limit the simulation time as much as possible.
5. The simulation runs generate a huge amount of output data which have to be evaluated by the software. An additional postprocessor is used to find critical stress cases and sort them by significance. This software part has to deliver a summary of results and find possible failures or incorrect runs.

3 Simulation approach

3.1 Simplified models

The modeling of the snapback curve's negative differential resistance (NDR) usually is associated with severe problems in convergence, numerical stability and simulation time (Zhang, 2001). A good example are 2 protection elements in parallel with a voltage drop around the triggering voltage. This state will force a normal simulator to decide which single element will jump into the snapback, and the decision may be arbitrary especially taking device variations into account.

The key to our method is the replacement of the compact model by a piecewise linear model of the protection element's IV characteristic with two or more independent model parts. For devices with diode-like character this description contains a Zener-Diode-like description with the corresponding resistances. Devices with a snapback will be represented by two Zener-diode-like devices in one model. Thus, each device has to be considered in its two possible states: breakdown (BD – device not triggered) and snapback (SP – device is triggered).

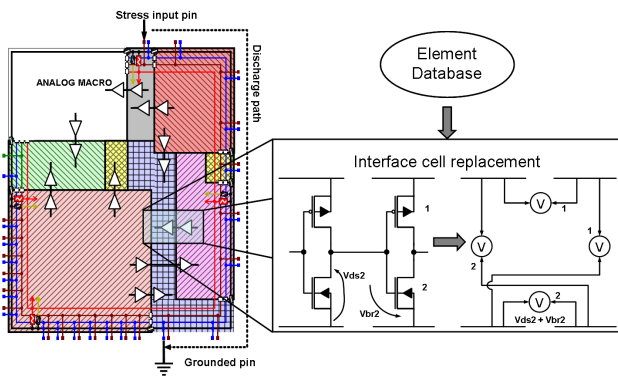


Fig. 2. Transformation of interface elements to combined voltage sensors in the corresponding critical paths.

As shown in Fig. 1 the model contains some physical impossible zones which are blocked by the parameters for the validity range in the model. Because there are two parts of these linear descriptions and starting the simulations it is not known in which state the device will be, all combinations of states have to be regarded.

3.2 Permutational approach – implementation

The permutational approach takes into account that devices could have two possible states and covers every combination of single device states. This simulation method will be necessary if more than one protection device reaches the trigger voltage and the DC simulation is used.

Thus, for finding every critical constellation the only safe solution is to try out every possible circuit state. The jump into snapback is only a very short temporary condition, which does not have to be modeled for finding the critical condition.

In the first simulation run every element is assumed to be in a non-triggered high ohmic state in order to detect all possible discharge paths. Afterwards the elements which exceed the breakdown voltage of the breakdown branch will be marked as permutation elements. The software will now perform additional runs with a permutational variation of the states of all marked devices. Physically impossible solutions arise e.g. when a voltage higher than the BD voltage arises at a device in BD state. They are rejected during validity check. Introducing a valid-criterion and a fail-voltage together with the basic circuit elements in the models it is possible to use every circuit simulator for the calculations.

3.3 Possible hot spots in the core

Possible victims for damage are interface devices between two or more voltage domains (Huh, 2005). In Fig. 2 a simplified product example is drawn with interfaces between different supply blocks. If this were a general problem it would

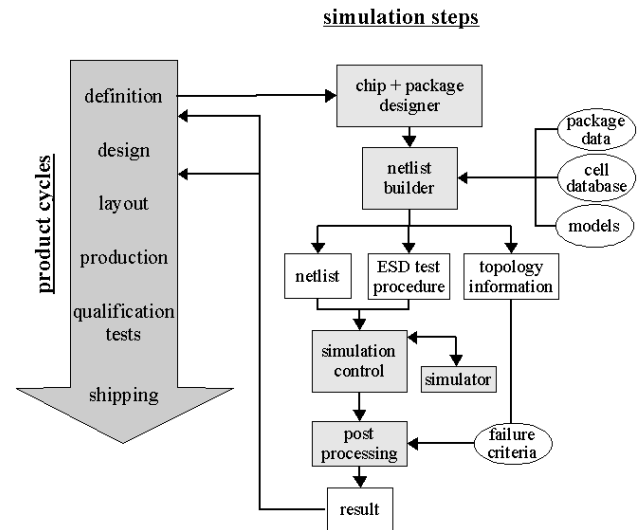


Fig. 3. Simulation flow and influence on development flow.

be covered during the place&route step by special rules. But such a scenario only happens with a certain small probability, especially together with adverse influence of the package, and is dependent on the interface devices.

In a worst case a sensitive gate oxide in such an interface device will receive the full voltage difference between two domains. This total voltage difference drops over the sender's channel (V_{ds2}) and the receiver's gate oxide (V_{br2}). By using voltage monitor cells with technology specific borders according to the device types the simulation tool can detect critical conditions, Fig. 2.

To track these constellations a special step is performed during the source data conversion which searches for interface elements between domains and checks their device types. For ESD simulations only one representative element of every device combination between two domains is sufficient to predict the ESD robustness. Equal combinations of devices between the same blocks will be considered as one kind of interface element.

3.4 Stressplan generation and simulation flow

International standards for ESD-qualification give strict guidelines for ESD-tests and how devices are to be stressed. A basic rule for two-pin stress is that every pin combination has to be stressed. In detail there are some differences between existing standards, but they resemble in the amount and order of discharges per combination. To reduce the testing efforts pins are sorted into groups and will be stressed depending on their group. Furthermore, for simulation issues it is not needed to simulate every stress combination, e.g. if the input or output pin is part of a low-ohmic package network with more than one pin.

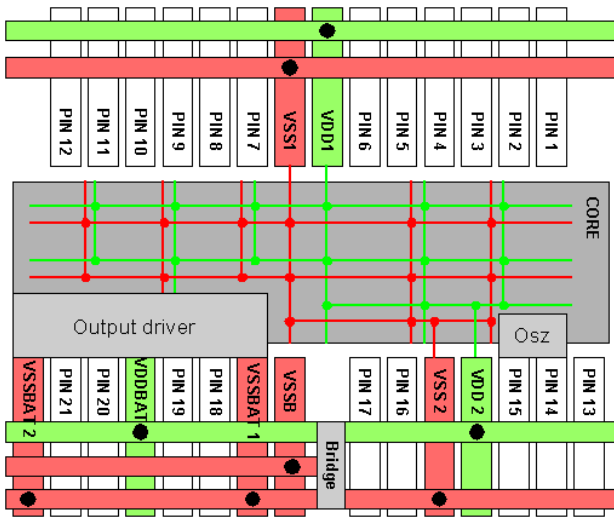


Fig. 4. Product example – layout and principle of pin configuration.

The whole simulation framework is divided into three separate parts (see Fig. 3). The first part generates the netlist and additional data for simulation control. The second main part contains the calculation routines for internal simulation, the control and the interface to the external simulator. The third part is used for the result interpretation.

The topology and design information from a chip/package co-design tool is combined in the ESD netlist builder with data taken from a library cell database. The netlist builder will provide the chip level ESD netlist, an ESD stress plan, i.e. a simulation job file containing all ESD test events as required by current test standards, and a topology data file needed for automated post-simulation analysis. The simulation driver will step through the stress plan and take care of the permutational simulation runs. The user can choose between the implemented circuit simulator and an external circuit simulator, e.g. SPICE.

3.5 Result processing

This simulation generates a huge amount of data which contains the voltage distribution and partial currents of every element along the current path and for every stress combination. A first and rough simulation result analysis can be done in the simulation driver based on the voltage sensors in the ESD netlist. Full data evaluation is performed by the simulation data post-processor. Based on the topology data file voltage drops over functional blocks are monitored and assessed. Current and voltage distributions in the I/O cell ring can be compiled, organized in various graphical views and displayed to the user.

4 Application example

As a proof of concept a simulation run on a real product was performed without additional extractions or reports from the design group.

4.1 Source of netlist information

Within the first step an existing pinlist for ESD-review is used to generate an ESD-netlist, a full stress plan and a file with topology information for the result processing. The subcircuits for padcells are created during library generation and reused for this simulation. The model files with the piecewise linear description of the protection elements are made for this technology and can be used for all products on this technology platform. The input data contains only padding data and abstract information on the core circuitry as is available in the earliest design steps.

4.2 Product description

This sample was a fully digital design with a custom-built output line driver block and an oscillator circuit. Figure 4 shows the simplified floorplan and power connectivity without signal lines.

This 28 pin IC uses a 90 nm standard CMOS process and has two voltage domains. As an additional challenge this chip does not have a closed padding and uses the core power mesh as connection between the two pad stripes. The core mesh for power and ground has to be added to the simulation netlist since it is part of the protection network. Every signal pin has protection elements and is connected to the shown rails for power and ground. The circuit has several control lines with additional protection elements from the digital core to the output driver block which are identified as interface elements and added to the simulation netlist. The bridge between the domains is required by the package. It contains additional protection elements and separates the domains.

4.3 Interface elements

The full IC netlist is used to find every network which is connected to two or more devices in different domains and replace them by voltage sensors. The fail voltage levels are calculated by the sum of the gate oxide breakdown voltage V_{br2} of the receiver and the threshold voltage V_{ds2} of the sender, as showed in Fig. 2. The search routine for interface elements found 10 common networks between the two domains. These networks are connected to 19 elements which could be simplified to two interface elements due to identical device types. The elements are added to the input pinlist as subcircuits including voltage monitors.

4.4 Netlist generation and simulation

The simulation netlist is generated in two steps by the software suite. First step is the extraction of interface elements and the generation of special subcircuit cells. The whole core mesh is divided into 22 subcircuits as equivalent circuits for the VDD- and VSS-metallization. The division of the core blocks follows product specific and geometrical aspects and leads to a combined subcircuit cell for power and ground network. Between the VDD- and VSS-networks there are high resistances as a substitute for currents during an ESD-pulse caused by capacitance charging. The simulation is controlled from a platform independent graphical user interface.

4.5 Simulation results

The full stressplan for the example product contains 538 stress combinations. A full simulation run at nominal stress conditions (HBM: 2 kV – 1.3 A) consumed about 4 h on a UNIX workstation cluster and generated no fail condition of any used device. Two additional simulation runs were performed for testing the applicability of this software to typical cases in product development. Based on the results of the real product ESD-test a new stressplan was generated. The new stressplan contains test combinations of a selected signal pin (Pin 21) against each power-, ground- and one signal-pin of both domains. During the ESD-test the IC was stressed accordant to the JEDEC-standard which stresses the IC first and performs current measurements afterwards.

4.5.1 Increased stress level

This simulation should check the product behavior for higher stress level. The ICs were subject experimentally to a HBM test with increased stress level (3 kV – 2 A) resulting in leakage current on output driver's signal pins and increased power consumption within the output driver. This implies a fail in a protection element of the signal pin.

The new simulation result showed some failures relating to the signal pins protection elements and the voltage monitors between the two domains. In Fig. 5 the voltage distribution within the VDD mesh is drawn and shows a significant voltage drop between the domains. The fail condition appear after stress combinations which cause a current path over the domain borders.

The failing protection element results in a hard error on an element between VDD.BAT and the stressed signal pin. A reason for this fail in the protection element might be a too weak protection element and a too high resistance in the VDD-VDD.BAT bridge. The resulting error would cause increased leakage current, as was measured in the real IC.

Furthermore the voltage monitor reports an overvoltage which indicates a possible gate oxide gate breakdown at the interface between the domains.

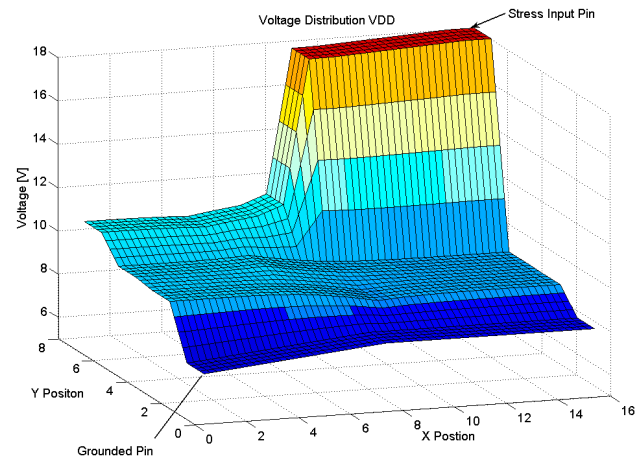


Fig. 5. Voltage distribution VDD mesh.

4.5.2 Required interface protection

A second simulation run with a modified input netlist and a HBM stress level of 2 kV was performed. In this version the additional protection elements at the domain border were removed. These protection elements are mandatory only in non-common ground packages. This simulation run emulates the situation if a design for non-common ground packages were used together with a common ground package.

Voltage monitors were retained at the positions of the removed interface protection elements. They showed warnings in several stress cases. The failure locations indicate a possible breakdown at the interface between domain VDD and VDD_BAT domains. The monitors produced the same voltage warning levels as before. The removed protection elements limited the voltage difference between the power networks in this location. By removing these elements the voltage difference was increased by about 2.5 V at this interface. This would cause a gate oxide breakdown of the involved transistors.

5 CDM simulation methodology

In contrast to specifically designed test circuits, an IC design on full chip level challenges by its high complexity. The proposed “CDM-alike” method adapts the combinational simulation method to extract the voltage levels of a worst case quasi static (DC) state.

The total chip area is normally densely filled by circuit parts. As the p-substrate silicon is connected to VSS and n-wells are connected to VDD, the charge present before the CDM discharge can be assumed to be on the metal layers.

CDM discharge is strongly dependent on package type and size (Brodbeck, 1998), as package represents an essential part of the discharge path and a charge source. The package

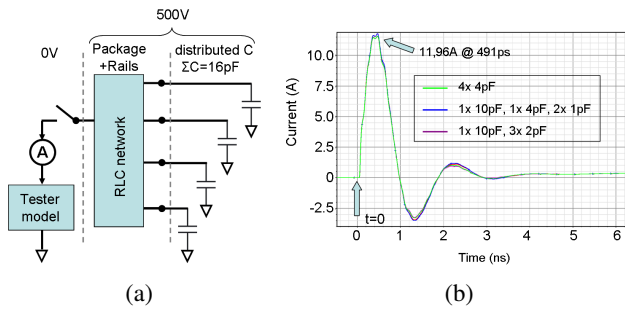


Fig. 6. Simulation setup for transient CDM simulation.

together with the ESD-test set-up determines the peak level and the shape of the discharge current to a large extent. The peak CDM current is generated by the distributed capacitors between the IC and the ground plane of the CDM-tester and flows through the testpin.

For transient simulations the distributed capacitors and the capacitances of the package model were charged to 500 V and discharged through the tester, modeled as shown in Fig. 6a. The total capacitance of 16 pF was divided into different combinations of 4 capacitors. The transient results, Fig. 6b, show no differences in peak level and shape of the discharge current through the testpin.

These results suggest a transformation of the CDM charge sources to constant current sources like shown in Fig. 7b. The known total peak current for a specific package is divided into several current sources. The strength of a single current source corresponds to the fraction of the external capacitance contribution of this point.

The final simulation netlist Fig. 7a includes the package and tester models and the ESD-relevant elements of the core area. This core netlist covers the IO-ring with pwl-models, a resistance network for the power and ground-meshes and voltage monitors on typical places. The capacitors within core and package are replaced by constant current sources, Fig. 7b. The sum of all current sources is equivalent to the known peak current of the used package. The voltage monitors will issue an alert if the voltage limit is exceeded.

The biggest advantage of this transformation is the fast and simple simulation setup and the concentration on results relevant for the product verification. The input data can be either abstract information available during floor-planning or extractions from the final layout. In the early design stages both the package and the IO-ring are already known.

The core mesh will be represented by typical resistance networks with a size conformal to the domain size. The voltage monitor limits depend on technology and already known topology of the IC. For simulations on the final layout the extracted netlist of power and ground meshes will be used for the core representation. The package model and the IO-ring model will be the same in both cases.

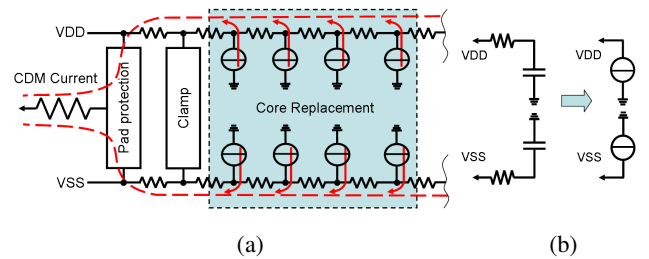


Fig. 7. Simulation setup for DC simulation (a) with transformation of capacitors to current sources (b).

6 Conclusions

Chip level ESD simulation has been shown to be a vital need in the design flow of ULSI circuits. It will assist in the ESD compliant setup of the overall ESD protection concept mainly determined by the correct layout of I/O cell ring, bond-out and package. A simulation flow and framework was presented that reduces modelling extraction and simulation efforts. The simulation covers possible failure locations and helps to assure the ESD-robustness of upcoming products. The presented ESD simulation methodology can be applied from the product concept phase until the final ESD-review. Three HBM simulation runs showed that the simulation software is able to reproduce realistic errors in the ESD-protection concept.

The presented “CDM-alike” approach satisfies the requirements for a CDM verification procedure during the IC design phase. With the transformation of capacitances to current sources it is possible to set up a fast and meaningful CDM simulation which delivers sufficient information to determine the CDM weaknesses of an IC design reliably. Even when only presented for simple examples these considerations show the direction a DC-simulation based verification for complex system on chip design can go.

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