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Proposal for scalable models in EMC simulation

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Abstract. In this paper a method "Component Series Modeling" (CoSeMod) is presented. This allows fast and easy implementation of scalable model generations for passive component series based on measurement data or specification provided by manufacturer. These can be used in circuit models for fast EMC analysis and optimization, especially in frequency ranges where conducted emission and susceptibility dominate. EMC tasks require high precision equivalent circuit models of components. Models generated with CoSeMod provide in many cases as high a quality as original (static) models do. One feature of scalability is that new netlisting is not needed after component changes. The process of model creation is based on similarities of the components of the same model series (packaging, manufacturing process, material etcetera). Required equations of the relationship between nominal and parasitic values are calculated by nonlinear regression. Model generation for unknown components of a known series is possible with interpolation. Implementation is possible with relatively simple actions made in circuit simulator Saber. An EMC application example of the implemented model is also shown in this paper.

1 Introduction

High quality but scalable models of components are needed in EMC optimization tasks to achieve realistic optimization results. Manufacturers of electronic components nowadays provide datasheets for the components or, in some cases, simulation models are available in standard format e.g. SPICE, MAST, VHDL-AMS. These models are 'static' in terms of representing only one component from a series according to the requirement of the customers. The parameters of the parasitic effects are, in the equivalent circuit, not dependent on other values. This means for an EMC behavioural optimization that there are two possibilities to use the existing models.

– If the parasitic effects are not considered in the optimization and only the main parameter of the component is optimized, the result of the optimization can be very implausible. Parasitic effects can significantly influence the spectral and transient character of a circuit. Usage of this method is restricted for that reason.

– If the models of every individual component with parasitic effects are considered, the models have to be swapped in the circuit schematic during optimization. A new netlist has to be generated after every iteration step and bias point values have to be calculated again. This is an appropriate method to obtain exact optimization results. Due to swaps and bias calculations the realization is very resource consuming and complicated.

Models delivered by manufacturers are not specified for HF or EMC analysis and they focuse on behavioural modelling of the component. It is recommended to use our own scalable models for whole component series in case of EMC optimization tasks.

Scalable models can be realized in circuit simulators from datasheet or measured data (e.g. Cojocaru et al., 2002). One possible realization is a subcircuit model with lookup table (LUT). LUT models have accurate results but several disadvantages downgrade usability: no good overview of relations, no adjustability, complicated realization, and no possibility to statistically correct modelling. Another possible solution is to build up the model by using simulators hardware description language. It is very time-consuming as well and it can lead – without enough coding experience – to errors.

The most appropriate modelling for EMC optimization can be, in many cases, the CoSeMod scalable modelling for component series. In this method an equivalent circuit is realized as a subcircuit. Values of the circuit elements are calculated from the nominal value of the given component with a fitted regression model (Seber and Wild, 1989). In this paper models for four different series are investigated with 0603 or 0805 size and with X7R or C0G dielectric material.

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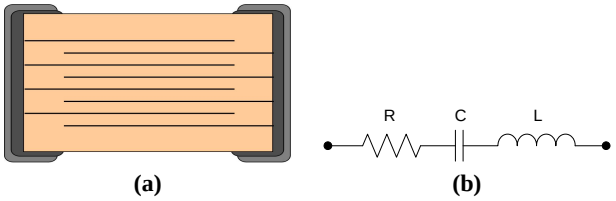


Fig. 1. **(a)** MLCC (multi-layer ceramic chip capacitor) structure **(b)** simplified equivalent circuit of MLCCs.

2 Theoretical background

The function of this method will be demonstrated on capacitors because of the relative simplicity of their construction but it is not restricted to them. Best modelling can be achieved if an accurate equivalent circuit is known and the parasitic element values are in strong correlation with the nominal value.

2.1 Modeling of capacitors

In monolithic ceramic capacitors the plates are stacked up in a comb-like structure in multiple layers as shown in Fig. 1 so the surface-to-volume ratio is large, and a ceramic material acts as the dielectric medium. Even if an accurate equivalent circuit of a MLCC involving parasitics is complex, it can be lumped as the simplest series or parallel circuit model, which represents the real and imaginary (resistive and reactive) parts of the total equivalent circuit impedance. Which circuit model should be used and which parasitic elements are determinative or negligible depends on the environment of operation, namely the applied frequency range and application. The goal was, in this case, to use the models in frequency ranges where conducted electromagnetic (EM) effects dominate. Usually, the frequency band for conducted emission measurements is 150 kHz–108 MHz in European countries (see in CISPR SC/D, 2008). However, modelling frequency range spans up to 1 GHz depending on the required accuracy. A realistic impedance characteristic is expressed with three-element RLC equivalent circuit parameters according to the required simplicity and fidelity. This structure is sufficiently accurate in most optimization cases; however the attenuation capability of the capacitor can be underestimated in noise reduction tasks, as described in Smith and Hockanson (2001).

2.2 Measuring impedance characteristic

Measurements were realized with a network analyzer equipped with 2000 µm HF probes. The DUT was placed on a rubber mat to avoid the influence of copper pad inductivity and to define a substrate for the measurements. In practical usage the substrate influence has to be considered also as in Lakshminarayanan et al. (2000). The test is demonstrated in Fig. 2. One port *S11* scattering parameter (Kurokawa, 1965)

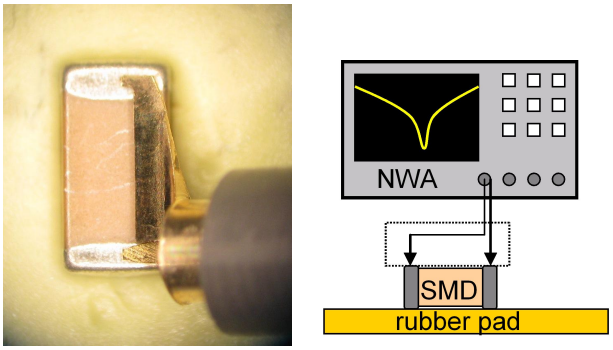


Fig. 2. **(a)** Measurement pins of HF probe on 0805 MLCC. **(b)** Test setup for impedance curve measurement with NWA.

measurement was carried out and the data was converted to get the impedance curve of the component based on the following equation:

$$Z_{11} = Z_0 \frac{1+S_{11}}{1-S_{11}} \tag{1}$$

Five pieces of the same component were measured. Components of one series were chosen by size, dielectric material, voltage limit, termination structure.

2.3 Model parameter extraction from measured impedance curves

The impedance curve can be split in three main regions. The capacitor behaves in the first region under series resonance frequency (SRF) as an ideal capacitor. So the impedance is determined by the following equation:

$$\log\left|Z_{(f<<\mathrm{SRF})}\right| = \log\frac{1}{2\pi f C} = \log\frac{1}{2\pi C} - \log f \tag{2}$$

At the resonance frequency there is no imaginary part of the impedance value so that the impedance is equal with the resistance of the circuit.

$$\log\left|Z_{(f=\mathrm{SRF})}\right| = R \tag{3}$$

Over the resonant point the inductive behavior dominates:

$$\log\left|Z_{(f>>\mathrm{SRF})}\right| = \log 2\pi f L = \log 2\pi L + \log f \tag{4}$$

From Eqs. (2) and (4) follows that a line with a slope of $\pm\log f$ has to be fitted on the measured data. L and C can be calculated from the y-value at the interception point of the y-axis.

As was mentioned previously, the investigated impedance curves of each capacitance value are an average of five measurements on five pieces of the same component. To perform a successful and reasonable regression on the dataset, the deviation of each curve can not be too large from the averaged

curve. Therefore the equivalent circuit parameters were extracted from each impedance curve and their standard deviation was expressed from the average value, on which the curve fitting will be performed later. The standard deviation of the interception parameter of the fitted straight lines during the parameter extraction was not taken into account since its value was negligible (less than 0,01%). Also the variability of values around the average is considered to follow approximately a Gaussian distribution. The investigation was performed on the smallest and the largest value for each capacitance range. The standard deviation of the ESC value is small and fits into the capacitance tolerance range given by the manufacturers (±5% for COG and ±10% for X7R). Also the equivalent inductance of the components shows an acceptable result, the standard deviation values are below ±5% in all cases. Notable differences can be observed only in the case of the ESR values. The measurement of the equivalent series resistance is less accurate for higher capacitance values with this measurement method, as described in Hajdu (2010).

2.4 Curve fitting with non-linear regression

Before performing the nonlinear regression, the appropriate model has to be selected. By taking a look at the shape or tendency of the data points, the main curve category that fits the results can be determined. However, at this step a trade-off has to be made between accuracy and simplicity. After defining the best model a first initial value for the model parameters is required to generate the first curve. To identify the fidelity of the model, the sum-of-squares is calculated. To reach predefined quality, the variables have to be adjusted to make the curve come closer to the data points. The goal is to minimize the sum of squared residuals:

$$\phi_{(x)} = \frac{1}{2}\sum_{i=1}^{m} f_i^2(x) = \frac{1}{2}\|F(x)\|^2 \tag{5}$$

Where $F : \mathbf{R^n} \rightarrow \mathbf{R^m}$ and $m \geq n$. Difference of the observed data point y_i and the calculated curve point at x_i is denominated as f_i where $\boldsymbol{\beta}$ is a vector of adjustable parameters.

$$f_i(x) = y_i - f(x_i;\boldsymbol{\beta}) \tag{6}$$

The most commonly used algorithm is the Levenberg-Marquardt method (Moré, 1978), which we also used. Some fitting quality indicators were used so that the quality of different fittings was comparable. The two indicators we used were adjusted R^2 and χ^2. The coefficient of determination, R^2 , can be calculated with the following expression with the mean of all observed data, $\bar{y}$:

$$R^2 = 1 - \frac{\sum_i (y_i - f(x_i;\boldsymbol{\beta}))^2}{\sum_i (y_i - \bar{y})^2} \tag{7}$$

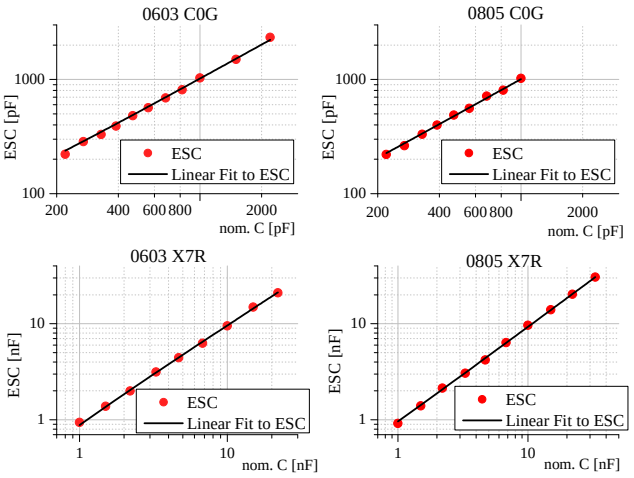


Fig. 3. The extracted ESC values and the results of curve fitting.

R^2 can be modified to adjusted R^2 to improve informative value with the sample size n and the total number of regressors k without the constant term in this form:

$$\text{adj.}R^2 = 1 - \left(1 - R^2\right)\frac{n-1}{n-k-1} \tag{8}$$

The errors can be assumed to have a normal distribution so that a reduced χ^2 distribution can be also used to test the quality of fit. The variance σ related to the measurement error for y_i is needed for the calculation of the reduced Chi-square.

$$\chi^2_{\text{red}} = \frac{\chi^2}{\nu} = \frac{1}{\nu}\sum_i \frac{(y_i - f(x_i;\boldsymbol{\beta}))^2}{\sigma^2} \tag{9}$$

The degrees of freedom (ν) can be calculated as $n-k$.

3 Fitting results

3.1 Equivalent series capacitance

The nominal capacitance of the measured DUT is dominant at lower frequencies. Therefore the data points resulting from the parameter extraction are expected to be very close to the nominal capacitance value. Figure 3 shows the corresponding curve fitting results for all the four types of capacitors with a linear regression. The outcome meets the previous expectations. The relation between the nominal capacitance of the DUT and the measured ESC values is linear.

The data points are plotted on a logarithmic scaled x- and y-axis, therefore the fitted curves also look linear.

3.2 Equivalent series resistance

To understand the series resistance of the capacitance we have to consider the structure of the component. The simplest interpretation is that the series resistance is the sum

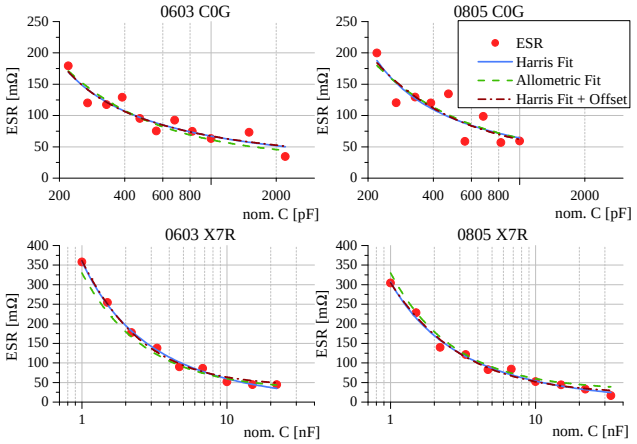


Fig. 4. The extracted ESR values and the results of curve fitting.

of the termination resistances and electrode resistances. A more sophisticated explanation can be found in Coda et al. (1976). Higher capacitance values can be reached with enlarging the overlapping area of the electrode plates, increasing the number of the plates, or with decreasing the distance between two electrodes. The last has negligible influence on the equivalent resistance; the other two reduce the resistance value. Thus one can expect that the resistance decreases with increasing nominal capacitance value. This expectation is confirmed by the measurement results in Fig. 4.

As there is no information about the internal structure of the capacitor, two standard fitting models were used for curve fitting: Allometric, Harris. They provide good quality and simplicity at the same time. The Harris fit gave a better result. An important aspect has to be taken into consideration. In the case of the two power form functions a reasonable meaning is behind their equations. The so-called Harris fit has a maximum value that it cannot exceed when the variable goes to zero. On the other hand, it does not have a minimum boundary so theoretically a DUT with large capacitance value can have zero ESR. This is obviously impossible. Therefore a modification on the Harris fit was necessary. By introducing a fourth parameter, the resulting function has boundaries for both extreme values. The outputs of the regression analysis for Harris fit with offset are collected in Table 1.

3.3 Equivalent series inductance

The most difficult parasitic component to measure and investigate is the equivalent series inductance. First of all it is performed at frequencies usually above 100 MHz so the imperfections in the measurement setup, the unwanted structural and external effects have extended influence on the accuracy. In addition, the value of the ESL in case of chip multilayer ceramic capacitors is quite small mainly due to the SMD packaging, and is usually around 0.5–1.5 nH.

Table 1. Curve-fitting results for the ESR values of the four different capacitors with Harris + offset.

	0603 C0G	0805 C0G	0603 X7R	0805 X7R
Eq.	$y = a + (b + c x_d) - 1$			
a	15	30	40	20
b	-0.02	-5×10^{-4}	5×10^{-4}	5×10^{-4}
c	0.01	3×10^{-5}	0,002	3×10^{-3}
d	0.23	1	1.2	1
Red. χ^2	230.9	585.3	78.2	128.7
Adj. R^2	0.85	0.73	0.99	0.98

The investigation of the measured results is also more complicated. To find out the source of ESL, again the structure of the chip multilayer capacitor shown in Fig. 1 should be inspected. The electrodes can be considered as flat metallic plates, whose thickness is negligible compared to the other two dimensions. Each elemental capacitor is in series with itself not only its own self-inductance, but also the mutual inductance of all the other plates, the magnitude of which will diminish with the plate spacing. As these spacings are generally small, these mutuals will approach, though never exceed, the self-inductance of any one plate. The inductance in series with each elemental capacitor will therefore not exceed nL. With n capacitors with L inductance in parallel, and since these can now be considered fully decoupled, the effective inductance of the whole capacitor will be the inductance of any one of them divided by n. This means that in case of the two extreme conditions, the resultant inductance does not change as the number of layers increases if the spacing between them is small enough. Or it decreases by $1/n$ if the electrodes are far from each other. Here the influence of mutual inductances between the terminals and the end of the opposite electrodes or between two parallel but not overlapping plates are neglected, since they are a lot smaller in value compared to those between the overlap region of the plates. Also the inductance of the terminals themselves has to be taken into account. To simplify the calculation, they can be considered to be constant for the investigated series of capacitances since the geometry of the SMD packaging does not differ to a great extent. As a consequence of the previously mentioned relationships, the ESL value of a chip multilayer ceramic capacitor is expected to decrease as the nominal capacitance increases, but because of the many influential parameters (plate geometry and number of layers) the correlation might be more complicated.

The previous expectations seem to be valid in most of the cases if we take a look at the fitted curves in Fig. 5 for all the four different capacitor types.

The distribution of the data points in case of the X7R type dielectric seems to follow a periodic behaviour. The origin of this behaviour is in a structure change between the values

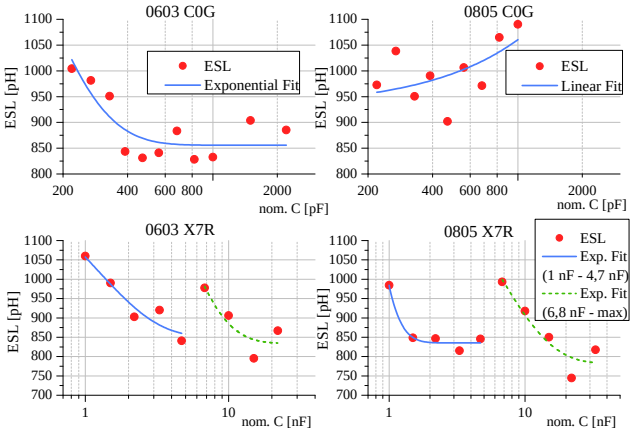


Fig. 5. The extracted ESL values and the results of curve fitting.

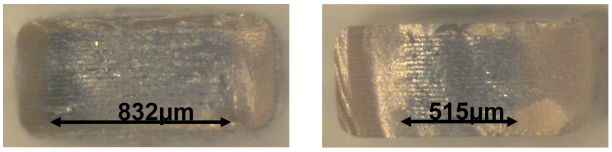


Fig. 6. Cross section view of 0805 X7R capacitances with **(a)** 4.7 nF and **(b)** 6.8 nF.

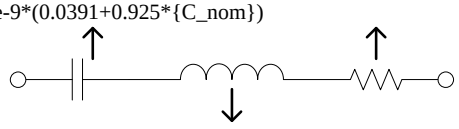
4.7 nF and 6.8 nF. The increased capacitance value is reached with an increased number of plates but their dimensions are lesser. This is depicted in Fig. 6.

Unfortunately no such behavior could be observed regarding the components with C0G type dielectric, although in the case of the 0603 sized DUT the data points are still not randomly scattered, so here the distribution was approximated also by an exponential function. For the 0805 sized C0G type capacitor, a reasonable fitting function could not be found, so a simple linear one was used.

4 Implementation of the model

To test the previously expressed equations of the scalable models they have to be implemented in a circuit simulator. The implementation was realized as a subcircuit in Saber. A little trick was needed because the compiler of Saber does not understand every mathematical operation. Therefore the implemented equations look a bit more complex, because the power operation was substituted by the combination of exponential and logarithm functions. The step in the ESL curve of X7R capacitors between 4.7 nF and 6.8 nF, which has been explained in Sect. 3.3, was realized by the use of the *int* command, which rounds the operand to the nearest integers towards minus infinity. Realization for the 0805 X7R capacitor (right bottom corner in Figs. 3–5) is in Fig. 7, where *C_nom* is the nominalvalue of the capacitor in nF.

```
rnom.r1=1e-3*(15+1/(5e-4+2.97e-3*exp(0.96*ln({C_nom}))))
c.c1=1e-9*(0.0391+0.925*{C_nom})
```



```
l.l1=1e-12*((835.3-(int(({C_nom}/(6.8+{C_nom}))+0.5)*53.8))+...
(17111.4-(int(({C_nom}/(6.8+{C_nom}))+0.5)*16411.6))*...
exp((-4.74+(int(({C_nom}/(6.8+{C_nom}))+0.5)*4.57))*{C_nom}))
```

Fig. 7. Subciruit realization of the scalable model for one 0803 size X7R capacitor.

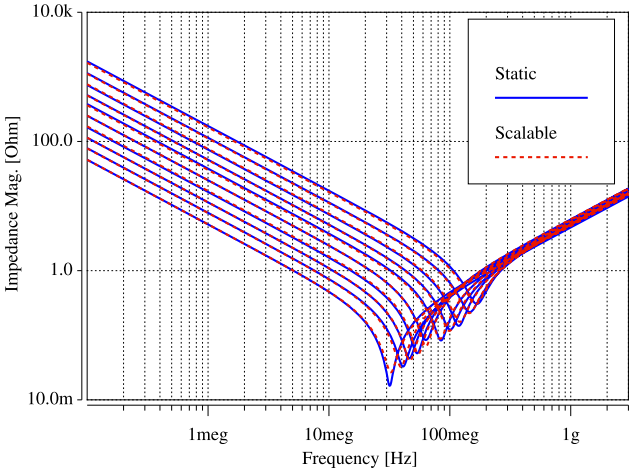


Fig. 8. Comparison of scalable and static model impedance magnitude for 0805 X7R capacitance series.

The scalable models were compared with the static models to validate them. The goal was to show that they are almost as good a quality as static models are. The comparison of the model shown in Fig. 7, is in Fig. 8.

The difference between the simulation and the measurement is quite small in the case of this series, but to have a better overview, the accuracy of each equivalent circuit parameter has to be tested. Therefore results of those capacitances were collected where the difference between the measured value and the fitted curve was the biggest. In this way the maximal margin can be determined and so the worst case situation can be investigated. The results are collected in Table 2. The accuracy is very high in all cases except in case the of the ESR. The measurement uncertainty of the resistance value also influences this result (see Sect. 3.2). This value is responsible for the amplitude in the spectrum which is measured usually in dB. For that reason this deviation is also acceptable for EMC purposes.

5 Possible usage in EMC

Scalable models are not avoidable if the goal is an automated EMC optimization, described in Leibinger (2010).

Table 2. Maximal modelling failures.

Parameter	ESC	ESR	ESL
0603 C0G	3.20%	15%	5.60%
0805 C0G	3.30%	22.10%	9.10%
0603 X7R	3.20%	14.40%	5.80%
0805 X7R	3.40%	13.00%	6.70%

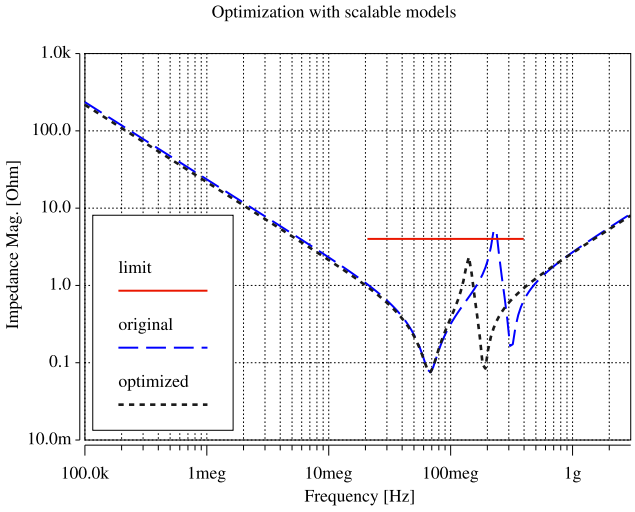


Fig. 9. Optimization of an input filter of two parallel SMD capacitors.

One typical task is the parameter optimization for input filters. In Fig. 9 is an example of two parallel 0603 size scalable capacitor models with X7R (1–22 nF) and C0G (220–2200 pF) dielectric for input filter optimization.

The advantageous behaviour of the scalable models is that they are easily extendable. With new functions within the subcircuit, more optimization goals can be defined simultaneously e.g. thermal, cost. The thermal or cost functions can be determined with the same method as the parasitics above.

6 Conclusions

Scalable models can be used in simulations, when a rapid optimization is desired. They reduce the number of parameters to be changed and therefore save computing capacity. Validation of the models must be proved with statistical measurement data if possible. A very good model approximationwith interpolation is possible for unknown components of one model series, which is presented with only few known components. This can be considered as a time-saving possibility for fast modelling. If a sufficient level of maturity is achieved in such models, these models can provide as good a quality as static models do for many component types. Good scalable modelling can be achieved with components in series that have little scattering regarding nominal value and parasitic values. SMD components are suitable for such a modelling.

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