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Countermeasures against NBTI degradation on 6T-SRAM cells

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Abstract. In current process technologies, NBTI (negative bias temperature instability) has the most severe aging effect on static random access memory (SRAM) cells. This degradation effect causes loss of stability. In this paper countermeasures against this hazard are presented and quantified via simulations in 90 nm process technologies by the established metrics SNM_{read}, SNM_{hold}, I_{read} and Write Level. With regard to simulation results and practicability best candidates are chosen and, dependent on individual preferences at memory cell design, the best countermeasure in each case is recommended.

1 Motivation

The ongoing miniaturization in modern CMOS technologies leads to a more and more challenging SRAM design: during read operation the cell must not flip to prevent data loss. During write operation the memory cell must flip to write new data in the cell. Thus there is only a certain area, where both a reliable read and write operation is possible. On top of variations, degradations are making this area smaller.

To illustrate the effect of variations and degradations on SRAM cells, a Monte Carlo analysis was performed (Fig. 1).

In this analysis 10^5 SNM_{read} simulations (Seevinck et al., 1987) are performed for $0.4\,V < V_{DD} < 1.2\,V$: the transistors are exposed to variations (based on measured σ values), then -50 mV NBTI degradation is added to one pullup transistor. This represents a realistic worst case, as the expected end-of-life shift after 10 years at 1.32 V and 125 °C is -31 mV. Counting the number of not functional SRAM cells ($SNM_{read} < 0$) the yield (fraction of functional memory cells) is determined. For the 256 Bit SRAM array it is assumed that the failure of one cell leads to the failure of the whole array. When the cells are only influenced by variations, the yield of the 256 Bit SRAM array decreases rapidly below $V_{D,min} = 0.75$ V. To design functional SRAM arrays despite variations, different assist techniques have been developed. In contrast to variations, degradations occur with increasing magnitude during operating time. The $V_{DD,min}$ value, where the yield of the 256 Bit array starts to decrease, rises from 0.75 V to $V_{D,min} = 0.8$ V when the SRAM array is exposed to variations plus -50 mV NBTI degradation. So $V_{D,min}$ is increased by approx. ΔV_{th}. $V_{D,min}$ would rise more if additional other degradations and/or a higher NBTI degradation were taken into account. As a result, countermeasures against NBTI are necessary to guarantee long-time operational SRAM cells. One first countermeasure is e.g. the Guard Band (Sect. 3.4), where V_{DD} is limited to a value above $V_{D,min}$ to assure that the cell is not operated with a V_{DD} with a high failure probability after degradation.

After describing the consequences of the NBTI degradation on the SRAM cell in Sect. 2, countermeasures against NBTI degradation are presented (Sect. 3) and the best candidates in terms of simulation results and practicability are chosen and compared to each other (Sect. 4). Depending on the individual preferences at memory cell design, the best countermeasure in each case is recommended.

2 Consequences of NBTI degradation on 6T-SRAM memory cells

BTI (bias temperature instability) degradation distinguishes between PBTI (positive BTI) and NBTI (negative BTI) degradation. NBTI affects pMOS transistors with negativ potential on the gate referred to the potential on source and drain (Fig. 2). NBTI weakens pMOS transistor: Positive charges arise in the gate oxide and the absolute threshold voltage $|V_{th}|$ rises. It is harder to turn the transistor on. NBTI can be modeled with a rise of $|V_{th}|$ by ΔV_{th}. PBTI influences nMOS transistors with high-k gate oxide, thus in process technologies under 65 nm. So NBTI has the most damaging effect for current technologies (Drapatz et al., 2009a).

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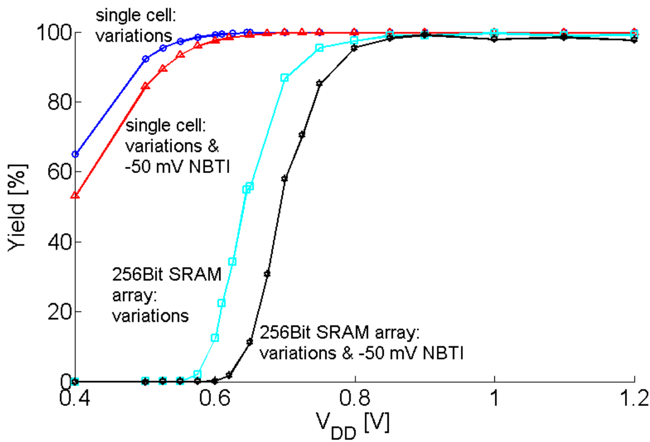

Fig. 1. Yield considering that the SRAM memory cell is exposed to variations and variations plus NBTI degradation of -50 mV, respectively for a single cell and a 256 Bit SRAM array. (based on 10^5 simulations). NBTI degradation increases $V_{D,min}$ (lowest voltage before the yield decreases rapidly) by approx. 50 mV.

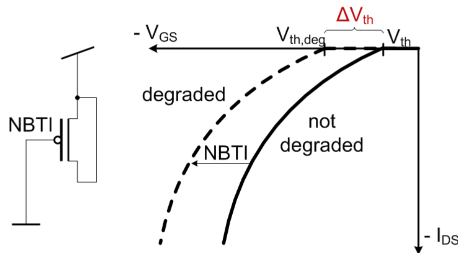

Fig. 2. Left: NBTI stress condition for single pMOS transistor; right: influence of NBTI: higher absolute threshold voltage. The degraded transistor is weaker.

By means of the NBTI-Calculator Formula, adapted to single transistor degradation measurements, the actual existing ΔV_{th} can be determined with a model based on Yan et al. (2009), Huard et al. (2010) with appropiate parameters for the used process technology.

$$|\Delta V_{th}| = A \cdot t^n \cdot V_{DD}^{V_0} \cdot \exp(-\frac{E_a}{kT}) \quad (1)$$

ΔV_{th} rises exponentially with increasing T, exponentially with increasing V_{DD} and with a logarithmic dependence on stress time t. For the used 90 nm pMOS transistor model the ΔV_{th} for the nominal point ($V_{DD} = V_{WL} = V_{BL(B)} = V_{DD,core} = 1.2$ V and $T = 25$ °C) is $\Delta V_{th} \approx -4$ mV after five years and $\Delta V_{th} \approx -5$ mV after ten years. For the realisic worst case point ($V_{DD} = V_{WL} = V_{BL(B)} = V_{DD,core} = 1.2\,\text{V} + 10\% = 1.32$ V and $T = 125$ °C) $\Delta V_{th} \approx -26$ mV after five years and $\Delta V_{th} \approx -31$ mV after ten years. ΔV_{th} will increase for future process technologies. $\Delta V_{th} = -100$ mV is chosen as a worst case value for this technology and the SPICE simulations are performed for ΔV_{th} between -100 mV and 0 mV.

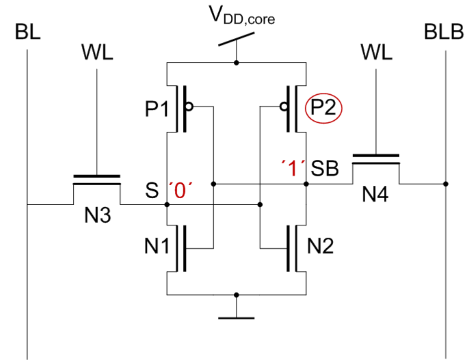

Fig. 3. NBTI stress condition in hold and read operation (the cell is in the “0" state (S: “0", SB: “1")) is only fulfilled for pMOS P2. In write operation the position of “1" and “0" switch, so P1 fullfills the stress condition.

Table 1. Metrics in the nominal point ($V_{DD} = 1.2$ V, $T = 25$ °C) for the non-degraded and the degraded cell (worst case: $\Delta V_{th} = -100$ mV): The most impact is on read stability.

	non-degraded cell $\Delta V_{th} = 0$ mV	degraded cell $\Delta V_{th} = -100$ mV
SNM_{read}	0.117 V	-0.016 V (-13.7%)
SNM_{hold}	0.388 V	-0.026 V (-6.7%)
I_{read}	6.598×10^{-5} A	-7×10^{-9} A (-0.01%)
Write Level	0.656 V	+0.039 V (+5.9%)

In this paper the established metrics SNM_{read}, SNM_{hold}, I_{read} and Write Level are used: SNM describes how much additional noise voltage is necessary to flip the cell. I_{read} is a measure for the speed of the read operation. Write Level describes the voltage necessary to flip the cell (Seevinck et al., 1987; Drapatz et al., 2009b).

In the hold and read operation, the SRAM cell is assumed to be in the “0" state (S: “0", SB: “1") (Fig. 3). So the NBTI stress condition is fulfilled for the pMOS transistor P2. In the write operation the positions of “1" and “0" switch and the stress condition is fulfilled for P1 after that.

Table 1 shows the metric values in the nominal point. The influence of NBTI on the writability (Write Level increases) and the read speed (decrease of I_{read} is small) is unproblematic. So the presented simulation results concentrate on the reduction of the stability.

3 NBTI countermeasures

3.1 Limited temperature

A decreasing temperature leads to improvement of the hold and read stability (0 °C, without considering ΔV_{th}: +1.8%, respectively +6.8%) and to lower ΔV_{th}. For $T = -100$ °C the

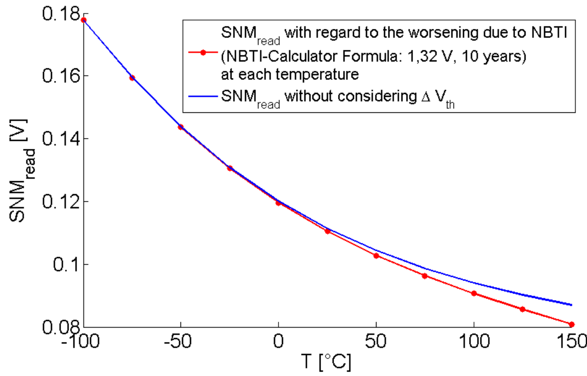

Fig. 4. Read stability over temperature considering both the simulation results at a constant ΔV_{th} and the potential rise of ΔV_{th} with V_{DD} (NBTI Calculator Formula, worst-case point). The lower the temperature, the higher the stability. So no optimal temperature limit can be determined.

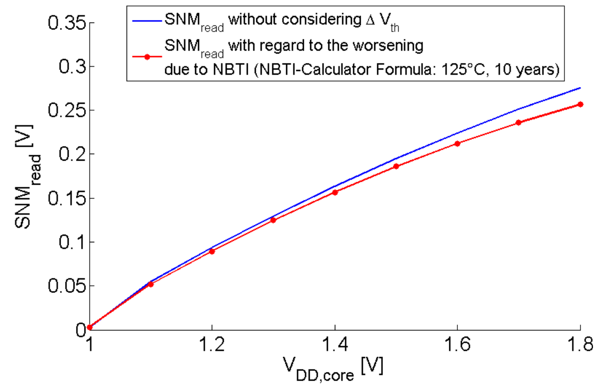

Fig. 5. Read stability over core voltage considering both the simulation results at a constant ΔV_{th} ($=0$ mV) and the exponentially rise of ΔV_{th} with V_{DD} (NBTI Calculator Formula, worst-case point). The higher the core voltage, the higher the stability. So no optimal core voltage can be determined.

Table 2. Metrics for various temperatures for the nominal point ($V_{\mathrm{DD}}=1.2$ V, 1 year). Percent values in comparison to the stability at 0 °C ($\mathrm{SNM}_{\mathrm{read},0\,°\mathrm{C}}$=0.125 V, $\mathrm{SNM}_{\mathrm{hold},0\,°\mathrm{C}}=0.394$ V). The most impact is on the read stability.

	50 °C	100 °	125 °C
$\mathrm{SNM}_{\mathrm{read}}$	0.109 V (−13%)	0.097 V (−23%)	0.091 V (−27%)
$\mathrm{SNM}_{\mathrm{hold}}$	0.381 V (−3%)	0.369 V (−7%)	0.363 V (−8%)

Table 3. Metrics for various core voltages for the nominal point (25 °C, 1 year). Percent values in comparison to $V_{\mathrm{DD,core}}=1.2$ V. The most improvement is on read stability.

	1.3 V	1.4 V	1.5 V
$\mathrm{SNM}_{\mathrm{read}}$	0.15 V (+25%)	0.18 V (+50%)	0.21 V (+75%)
$\mathrm{SNM}_{\mathrm{hold}}$	0.41 V (+5%)	0.42 (+8%)	0.44 (+13%)

degradation formula would yield $\Delta V_{\mathrm{th}} \simeq 0$ mV, so the pMOS transistors would not be degraded by NBTI. This is however far away from the operating conditions, where the measurements for fitting of the formula were performed, and an operating temperature $T=-100$ °C is not practicable anyhow. But in general it has to be considered that at higher temperatures the cells are less stable. So one can limit the temperature, although this narrows down the SRAM operating range (compare Table 2 and Fig. 4). Additionally, the NBTI degradation is getting worse with higher temperature. This can be seen in Fig. 4, when a second plot was added to the nominal plot. It considers an NBTI-related ΔV_{th} (worst case, calculated for 10 years at 1.32 V) that occurs due to the increased temperature. For this voltage and time the decrease in stability by raised T is so large that the NBTI degradation, also increased with T, does not affect the result much. It is not possible to determine an optimal temperature limit (Fig. 4): The lower T, the higher is the stability. So one must choose a suitable temperature limit for each particular case (e.g. Table 2, values given for the nominal point).

3.2 Core boosting

The stability is improving with increasing core voltage $V_{\mathrm{DD,core}}$: For e.g. 1.5 V instead of 1.2 V core voltage, the read stability can be improved by 75% (compare Table 3 and Fig. 5). On the other hand, it is important to note that the NBTI degradation is getting worse with higher $V_{\mathrm{DD,core}}$. This is shown in Fig. 5, where again a second plot was added to the nominal plot. It considers an NBTI-related ΔV_{th} (worst case, calculated for 10 years at $T=125$ °C) that occurs due to the increased $V_{\mathrm{DD,core}}$. For this temperature and time the increased stability by raised $V_{\mathrm{DD,core}}$ is so large that the also increased NBTI degradation does not affect the result much. It is not possible to determine an optimal $V_{\mathrm{DD,core}}$ (Fig. 5): The higher $V_{\mathrm{DD,core}}$, the higher the stability. But higher $V_{\mathrm{DD,core}}$ is also associated with higher power dissipation and greater leakage current. So one must choose a suitable $V_{\mathrm{DD,core}}$ for each particular case (e.g. from Table 3, values given for the nominal point).

To implement the Core Boosting, an additional voltage is necessary to supply the SRAM memory cell.

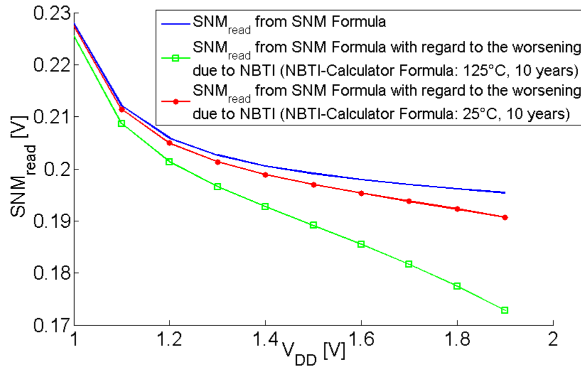

Fig. 6. Read stability over V_{DD} considering both the simulation results at a constant ΔV_{th} and the potential rise of ΔV_{th} with V_{DD} (NBTI Calculator Formula). The larger V_{DD}, the smaller the read stability. So no optimal V_{DD} can be determined.

3.3 Burn-In

Circuits that fail after short operating time are typically affected and weakened by variations. To prevent failures of those circuits in the field, Burn-In is typically used to make those circuits fail before they go to the customer. This is achieved through applying higher supply voltage and temperature for a defined period. Burn-In can be adopted as a NBTI countermeasure in the sense of pre-aging: If a specific ΔV_{th} can be achieved directly after production, ΔV_{th} increases only a little bit over the operating time, because ΔV_{th} rises with a logarithmic dependence over time. ΔV_{th} is approx. 5 mV after operating the cell 10 years at $V_{DD} = 1.2$ V and $T = 25$ °C. To achieve $\Delta V_{th} \approx -5$ mV during assembly, a Burn-In step at e.g. 2 V and 175 °C for 5 s would be necessary. The SRAM cell is centered without the Burn-In, i.e. in matters of stability and writability the cell has the best possible performance. After the Burn-In, the cell is not centered anymore. To achieve both, best possible performance and the use of Burn-In, the cell has to be adapted. For the example above, the width of the pMOS transistors need to be increased from 120 nm to 125 nm (required area rises by approx. 1%). Now the enhanced SRAM cell has the same performance at $\Delta V_{th} \approx -5$ mV (because of Burn-In) as the non-enhanced cell at $\Delta V_{th} = 0$ mV. The exact Burn-In and Enhancement parameters must be chosen for each particual case in subject to the desired accuracy.

3.4 Guard band

Below $V_{D,min}$ there is a drastic yield drop, i.e. safe operation is not possible (Fig. 1). So the minimal V_{DD} is limited to a value above $V_{D,min}$. $V_{D,min}$ depends on the existing degradation and variation and on the size of the SRAM array. As a result the limitation of V_{DD} narrows down the operating range. This is detrimental, especially for the hold operation, because there V_{DD} is typically lowered to reduce leakage current and power consumption. Nevertheless, the Guard Band is the up-to-date countermeasure in industry for all kinds of degradation, because it is easy to implement. An optimal V_{DD} limit must maximize the operating range and ensure good performance. To measure the performance the results of the SNM Formula (Seevinck et al., 1987) at constant ΔV_{th} and the exponentially rise of ΔV_{th} with V_{DD} were taken into account (Fig. 6): The greater V_{DD}, the smaller the read stability, where the slope increases below $V_{DD} = 1.2$ V. When V_{DD} is lowered from 1.2 V to 1 V, the read stability improves by approx. 11%), but read speed, hold stability and writability weaken. In summary an optimal V_{DD} border must be determined for each particular case.

Table 4. Metrics for various wordline voltages for the nominal point ($T = 25$ °C). Percent values in comparison to $V_{WL} = 1.2$ V. The read stability is improved, but read speed and writability decrease.

	0.7 V	0.9 V	1 V
SNM_{read}	0.286 V	0.218 V	0.184 V
	(+144%)	(+86%)	(+57%)
I_{read}	2.4×10^{-5} A	4.1×10^{-5} A	4.97×10^{-5} A
	(−64%)	(−38%)	(−25%)
Write Level	0.148 V	0.35 V	0.447 V
	(−77%)	(−47%)	(−32%)

3.5 WL Boosting

WL "Boosting" actually means a lower WL voltage to improve read stability. For e.g. $V_{WL} = 0.7$ V instead of 1.2 V the read stability can be improved by 144% (the hold stability remains unchanged). On the other hand, read speed and writability worsen by 64% and 77%. (Table 4). It is not possible to determine an optimal V_{WL}, because there is an approx. linear relation between each metric and V_{WL}. So one must choose a suitable V_{WL} for each particular case (e.g. from Table 4, values given for the nominal point). It is also possible to implement different WL voltages during read and write, but at the cost of increased complexity of the peripheral circuits. In any case, an additional voltage is necessary to supply the WL driver circuits.

3.6 Symmetric degradation

The NBTI stress condition is fulfilled only for the pMOS of the "1" side of the cell. Long hold of this "1" lets the cell become assymmetric: P2 is degraded, while P1 is new. The intension of the symmetric degradation is to avoid this asymmetry by forcing a symmetric degradation of the cell. For this, the save state is re-programmed after a certain time to ensure that both pMOSFETs experience the same ΔV_{th}. This countermeasure is not expedient, because due to the logarithmic dependence on stress time the difference between

symmetric and asymmetric cells is small. But considering a NBTI degradation with recovery characteristic (Drapatz et al., 2010), that is not considered in this paper, this countermeasure potentially may lead to a higher improvement.

3.7 Lower precharge level

In read operation the node of the “0" side rises. As a consequence, it is easier to flip the cell. As a countermeasure one can lower the precharge level of the “0" side bitline. But in practice it is not possible to just lower the precharge level of the “0" side, because the position of “0" is unknown before the read operation. The only possible implementation is the lowering of the overall precharge level. However, a lower precharge level of the “1" side leads to an easier flipping of the SRAM cell during read. If the overall precharge level is lowered, the weakening of the “1" side node voltage is greater than the improvement of the “0" side node voltage: At $\Delta V_{th} = -100$ mV and $V_{BL,precharge} = 0.7$ V the node voltage of the “0" side increases from 0 V to 0.202 V and at $V_{BL,precharge} = 1.2$ V the voltage increases by additional 0.004 V to 0.206 V. At $\Delta V_{th} = -100$ mV and $V_{BL,precharge} = 0.7$ V the node voltage of the “1" side decreases from 1.2 V to 1.02 V, whereas at $V_{BL,precharge} = 1.2$ V the voltage decrease is only 1.198 V, i.e. 0.178 V less than at $V_{BL,precharge} = 0.7$ V. The simulations of the read stability confirm this result: SNM_{read} decreases by approx. 25% at $V_{BL,precharge} = 0.7$ V. The read stability is not improved, so lowering the precharge level is not expedient.

3.8 Alternative SRAM design: 8T, 6T with 8T size ratio

In read operation the 6T-SRAM cell experiences a read stability problem, because the node of the “0" side sees strong disturb: If the node voltage of the “0" side reaches V_{th} of the pulldown transistor of the “1" side, the node voltage of the “1" side is lowered. As a consequence the “0" of the “0" side can be overwritten by a “1".

The 8T-SRAM cell (Fig. 7) ensures a read-disturb-free operation, because this read stability problem does not exist. Data output and data retention are separated from each other via separate read and write signal lines. So the 8T cell is as stable in the read operation as the 6T cell in the hold operation. The required area for the 8T-SRAM cell is approx. 30% bigger than the area for the 6T design due to 2 additional transistors (Zhang, unpublished data; Bauer, 2009). During write operation, the 8T-SRAM array is disturbed by a parasitic read operation. The voltages of the wordline and bitlines of the 6 core transistors of the 8T cell for the half-selected columns in write operation are identical to the voltages of the 6T cell in read operation (Fig. 7). As a result the half-selected columns experience the same loss of stability in the write operation as the 6T cell in read operation. To prevent this loss of stability and the potential data loss, an array architecture without a bitline multiplexer is needed, where all cells connected to the same wordline are written at the same time. This mux-free array architecture leads to further increase of the required area (Bauer, 2009).

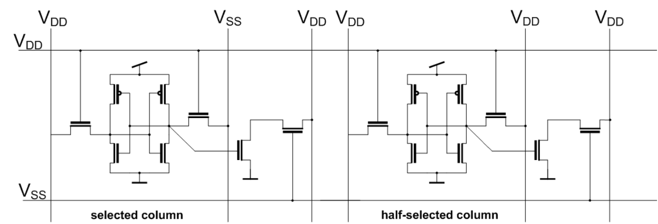

Fig. 7. 8T-SRAM memory cell write operation for the selected (left) and the half-selected (right) column. The half-selected column experiences the same loss of stability as the 6T cell in read operation, due to a parasitic read operation.

Another countermeasure is an enhanced 6T-SRAM cell. If e.g. a 6T cell with the same area requirements as the 8T cell is chosen, the read and hold stability increase by approx. 15% and 3%. The increase of the stability is smaller for the enhanced 6T cell than for the 8T cell. So in comparison to the 8T-SRAM design the enhanced 6T cell is not expedient.

3.9 Body biasing

The absolute threshold voltage $| V_{th} |$ rises, because of the NBTI degradation. With decreasing bulk-substrate voltage $V_{BS} < 0$ the pMOS threshold voltage V_{th} decreases (von Arnim et al., 2005). So with $V_{BS} < 0$ the rise of $| V_{th} |$ can be reversed: For $V_{BS} = 0.7$ V and $\Delta V_{th} = -50$ mV the SRAM memory cell has the same metric values as for $V_{BS} = 1.2$ V and $\Delta V_{th} = 0$ mV. For greater ΔV_{th} the stability and read speed is increased and the writability is decreased. The choice of a particular body biasing voltage must be fitted to the occuring ΔV_{th}. Besides it is possible to rise V_{BS} only in read and/or hold operation. Although this leads to a varying V_{BS}. So the great capacitance of the n-well must be transhipped depending on the operating state.

4 The best NBTI countermeasures

With regard to our simulation results and practicability, Core and WL Boosting, Burn-In, 8T-SRAM design and Guard Band are chosen as the best NBTI countermeasures. They are compiled in Table 5 and compared to each other in the following. The 8T-SRAM design is the most useful NBTI countermeasure: The stability problem of the 6T-SRAM cell does not occur anymore, but 2 additional transistors (required area is approx. 30% greater) are needed. The Burn-In ensures that ΔV_{th} only rises a little during operating time by an additional assembly step at higher T and V_{DD}. So the stability is approximately constant and the SRAM memory cell stays functional over operating time. The required area rises by approx. 1%, because the pMOS transistors must be

Table 5. Summary of the best NBTI countermeasures, numerical results for a 90 nm technology.

Countermeasure	Result	Positive aspects	Negative aspects
Core Boosting ($V_{DD,core} = 1.5$ V, nominal point)	SNM_{read}=0.21 V (+75%) SNM_{hold}=0.43 V (+13%) $I_{read} = 6.99 \times 10^{-5}$ A (+6%) Write Level = 0.55 V (+17%) determine optimal $V_{DD,core}$ for each particular case,	increase of stability, easy to implement	decrease of writability, additional voltage to supply cell, greater $V_{DD,core}$ ⇒ increase of power consumption/leakage current
WL Boosting ($V_{WL} = 0.7$ V, nominal point)	SNM_{read}=0.29 V (+144%) SNM_{hold} unchanged $I_{read} = 2.4 \times 10^{-5}$ A (−64%) Write Level = 0.15 V (−77%) determine optimal V_{WL} for each particular case,	increase of read stability, easy to implement, decrease of V_{WL} ⇒ decrease of power consumption/ leakage current	decrease of writability, decrease of read speed, additional voltage to supply cell
Burn-In	pMOS widened by 5 nm ⇒ size ratio rises by approx. 1%, choose Burn-In for each particular case e.g. for operation by $V_{DD} = 1.2$ V $T = 25$ °C: 5 s at 2 V and 175 °C	Over operating time: ΔV_{th} decreases only little ⇒ stability remains more or less constant	enhance of the cell ⇒ size ratio rises by approx. 1%, additional manufacturing step
Guard Band	determine optimal V_{DD} for each particular case e.g. $\Delta V_{th} = -50$ mV, 256 Bit SRAM array: $V_{D,min} \approx 0.8$ V	easy to implement (just border V_{DD}), up-to-date countermeasure	greater V_{DD} ⇒ increase of power, consumption/leakage current, narrows down operating range
8T SRAM Design	size ratio rises by approx. 30%, compared to 6T, read-disturb-free operation	separate read- & write signal lines ⇒Separation of data output and -retention	mux-free array architecture, increase of size-ratio by approx. 30%

widened. For implementation of the Core and WL Boosting an additional voltage (plus additional periphery and wire connection) to supply the cell is necessary in each case. Both countermeasures increase the read stability. The Core Boosting also increases the hold stability. The WL Boosting deteriorates the writability and read speed, while the Core Boosting leads to higher power consumption and greater leakage current. An optimal $V_{DD,core}$ or V_{WL} respectively, can not be chosen because of the approximately linear dependence of the metrics. So a suitable voltage must be chosen for each particular case. It is not recommended to implement the Core and the WL Boosting at the same time, because three voltages to supply the array would be needed. The Guard Band is the easiest countermeasure in terms of implementation: Only the miminmal V_{DD} must be guarded to be above $V_{DD,min}$. This narrows down the operating range of the SRAM and increases power consumption and leakage current. A suitable minimal V_{DD} must be chosen for each particular case.

5 Summary and conclusions

In this paper countermeasures against NBTI degradation that mostly impacts the stability of the cell were presented. With regard to simulations results and practicability the best candidates were chosen and compared to each other. Because it is not possible to define an optimal countermeasure, the best countermeasure, depending on the individual preferences in memory design, is recommended as follows:

1. *Area is not the first priority:* 8T SRAM Design
2. *Additional expenses during assembly is okay:* Burn-In
3. *Additional expenses for additional periphery and wire connection is acceptable:* WL or Core Boosting
4. *No design-change of the cell is preferred:* Guard Band

References

Bauer, F.: A Design Space Comparison of 6T and 8T SRAM Core-Cells, in: 18th International Workshop PATMOS 2008, 10–12 September, Revised Selected Papers, Lecture Notes in Computer Science, pp. 116–125, 2009.

Drapatz, S., Fischer, T., Hofmann, K., Amirante, E., Huber, P., Ostermayr, M., Georgakos, G., and Schmitt-Landsiedel, D.: Fast stability analysis of large-scale SRAM arrays and the impact of NBTI degradation, Solid-State Circuits Conference, ESSCIRC 2009, 35th European, pp. 92–95, 2009a.

Drapatz, S., Georgakos, G., and Schmitt-Landsiedel, D.: Impact of negative and positive bias temperature stress on 6T-SRAM cells, Adv. Radio Sci., 7, 191–196, doi:10.5194/ars-7-191-2009, 2009b.

Drapatz, S., Hofmann, K., Georgakos, G., and Schmitt-Landsiedel, D.: Impact of fast-recovering NBTI degradation on stability of large-scale SRAM arrays, Solid-State Device Research Conference, ESSDERC 2010. 40th European, 2010.

Huard, V., Chevallier, R., Parthasarathy, C., Mishra, A., Ruiz-Amador, N., Persin, F., Robert, V., Chimeno, A., Pion, E., Planes, N., Ney, D., Cacho, F., Kapoor, N., Kulshrestha, V., Chopra, S., and Vialle, N.: Managing SRAM reliability from bitcell to library level, in IRPS, IEEE International, 2010.

Seevinck, E., List, F. J., and Lohstroh, J.: Static Noise Margin Analysis of MOS SRAM Cells, IEEE Journal of solid-state circuits, SC-22(5), 748–754, 1987.

von Arnim, K., Borinski, E., Seegebrecht, P., Fiedler, H., Brederlow, R., Thewes, R., Berthold, J., and Pacha, C.: Efficiency of Body Biasing in 90-nm CMOS for Low-Power Digital Circuits, IEEE Journal of Solid-State Circuits, 40(7), 1549–1556 , 2005.

Baoguang Yan, Qingguo Fan, Bernstein, J. B., Jin Qin, and Jun Dai: Reliability simulation and circuit-failure analy- sis in analog and mixed-signal applications, Dev. and Mat. Rel., IEEE Transactions on, 9(3), 339–347 , 2009.

Zhang, M.: Performance Comparison of SRAM Cells Implemented in 6, 7 and 8-Transistor Cell Topologies, Electrical and Computer Engineering, University of California, Davis, unpublished data.