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Reliability analysis of buffer stage in mixed signal application

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Abstract. This paper discusses reliability analysis of a buffer circuit targeted for an analog to digital converter application. The circuit designed in a 32 nm high-κ metal gate CMOS technology was investigated by circuit simulation and sensitivity analysis. This analysis was conducted for realistic time varying (AC) stress. As aging effects, negative and positive bias temperature instability, conducting and non-conducting hot carrier injection are taken into consideration. The aging contributions of these effects on the different transistors in the buffer circuit and on different buffer performance figures are evaluated. Using these results, the impact of an aged buffer circuit on the performance of a successive approximation ADC circuit is evaluated. The most severely affected performance due to aging is amplifier offset, which leads to time varying gain error in the ADC circuit.

1 Introduction

Non-constant field scaling in nanoscale CMOS technology has led to undesirable reliability issues due to effects such as Negative Bias Temperature Instability (NBTI), Positive Bias Temperature Instability (PBTI), Conducting and Non-Conducting Hot-Carrier Injection (HCI,NCHCI). Significant device level research is carried out on these effects (Grasser et al., 2007; Kaczer et al., 2009). However, since the superposition of these effects in a circuit is quite complex, the study of their impact on circuit level is still in a preliminary stage (Jha et al., 2005; Martin-Martinez et al., 2009; Chouard et al., 2010a).

This paper targets to investigate the impact of aging on a buffer stage designed for Analog to Digital Converter (ADC) application. The circuit was implemented and simulated using 32 nm high-κ metal gate regular V_{th} nMOS and pMOS devices (Chen et al., 2008), so the effect of PBTI which appears due to high-κ is also present. The effects of buffer circuit degradation on ADC performance is demonstrated and the need for countermeasures is highlighted. The degradation effects are evaluated using a combination of sensitivity analysis and circuit simulation. This methodology as described in (More et al., 2010) was developed, as it needs considerably less computing effort than sole use of circuit simulation, and it provides more intuitive insight into the various degradation contributions.

Section 2 presents the models used for aging simulation. The investigated buffer circuit topology is shown in Sect. 3. Section 4 discusses results of aging simulation of buffer circuits. The analytical evaluation of these degradation effects using sensitivity analysis, its comparison with simulation results and the observed impact on the circuit performance are presented in Sect. 5. Effects of buffer circuit aging on ADC performance and need of countermeasures are discussed in Sect. 6. A conclusion is given in Sect. 7.

2 Modeling of device degradation

Device degradation due to aging resulting from NBTI or PBTI mainly shifts the threshold voltage (V_{th}) of MOS transistors, whereas HCI and NCHCI reduce the transistor current (I_d) and also give a smaller contribution to the threshold voltage shift. This can be modeled by replacing the MOSFET with an equivalent circuit shown in Fig. 1. The V_{th} shifts are modeled by an equivalent voltage source vt_{shift} in series to the gate terminal, the hot carrier effects by a current controlled current source (CCCS) Id_{shift} between the drain and source terminal. The threshold voltage shift by each of the BTI effects can be modeled by $(\Delta V_{th})_{\text{BTI}}$ as in Eq. (1). BTI stands for NBTI in pMOS transistors and for PBTI in nMOS transistors. The current degradation is modeled by

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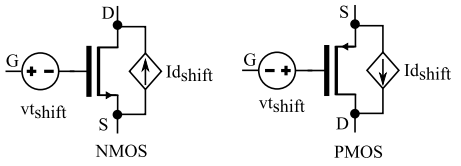

Fig. 1. Models for MOSFETs with degradation.

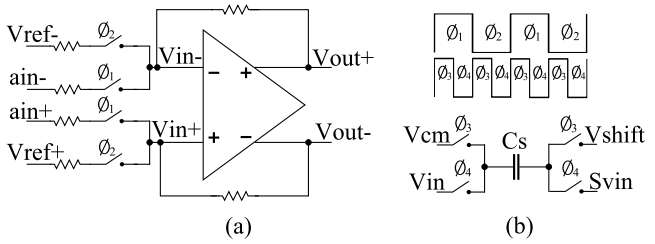

Fig. 2. Schematic of buffer and DC level shifting circuit.

Eq. (2), separately for HCI and NCHCI. The values of the equivalent sources are determined using Eqs. (1)–(2), which describe the relation of different contributing factors to the overall degradation, similar to (Martin-Martinez et al., 2009; Huard et al., 2009). The total vt_{shift} is the sum of two contributions, see Eq. (3). The total current degradation is modeled by Eq. (4). The model parameters were fitted to single device stress measurements.

$$(\Delta V_{th})_{\text{BTI}} = A \cdot \left(\frac{V_{gs}}{T_{inv}}\right)^{m} \cdot e^{\left(\frac{\Delta E}{kT}\right)} \cdot L^{\alpha} \cdot W^{\beta} \cdot t^{n} \tag{1}$$

$$(\Delta I_d)_{\text{HCI/NCHCI}} = I_d \cdot B \cdot V_{ds}^{p} \cdot e^{\left(\frac{\Delta E}{kT}\right)} \cdot L^{\delta} \cdot t^{q} \tag{2}$$

$$vt_{\text{shift}} = a \cdot (\Delta V_{th})_{\text{BTI}} + b \cdot (\frac{\Delta I_d}{I_d})_{\text{HCI}} \tag{3}$$

$$Id_{\text{shift}} = c \cdot (\frac{\Delta I_d}{I_d})_{\text{HCI}} + d \cdot (\frac{\Delta I_d}{I_d})_{NCHCI} \tag{4}$$

For the evaluations based on circuit simulation and to account for time varying (AC) stress, the aging simulation tool RelXpert$^{\text{TM}}$ (RelXpert, 2010) was used, which employs the above discussed models.

3 Buffer circuit for ADC application

The schematic for the fully differential buffer circuit is illustrated in Fig. 2a. It basically consists of an Operational Transconductance Amplifier (OTA), resistors and switches. Capacitors of 2 pF are used to emulate the load of a Digital to Analog Converter (DAC) connected at the output of

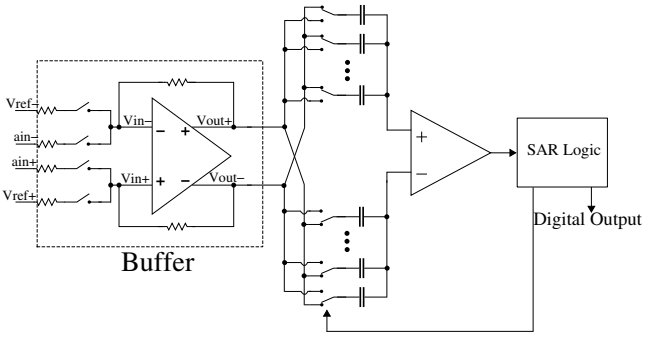

Fig. 3. Schematic of successive approximation ADC.

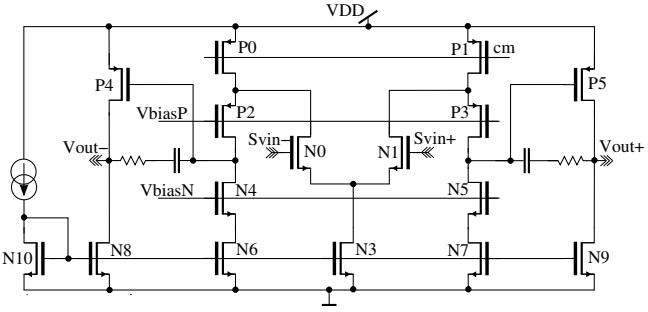

Fig. 4. Schematic of the OTA circuit.

the buffer circuit. The primary function of this buffer circuit in the charge distribution based successive approximation (SAR) ADC as depicted in Fig. 3 (Fulde et al., 2009), is to drive the DAC implemented using capacitors, within a short settling time (≈4 ns) with reference voltage ($V_{\text{ref}}\pm$) and analog input ($a_{\text{in}}\pm$) during different phases of the clock signals that control the switches. The clock signals are shown only schematically, not displaying the more complex clocking during the ADC operation.

The used OTA is illustrated in Fig. 4. It is a two stage folded cascode amplifier with Miller compensation. Implementing this circuit using regular V_{th} pMOS and nMOS transistors with $V_{th} \approx 0.45\,\text{V}$ and supply $V_{DD} = 1\,\text{V}$ leads to significant challenges in using the common mode voltage $V_{\text{cm}} = 0.5\,\text{V}$ at the gate of input differential pair (N_0 and N_1) and maintaining the tail transistor (N_3) in saturation. To overcome this problem a simple level shifting circuit as depicted in Fig. 2b was used at the input of the OTA. This circuit shifts each input signal (V_{in}) of the OTA with $V_{\text{cm}} = 0.5\,\text{V}$ to a new shifted signal (S_{vin}) depending on the difference between the common mode and the shift voltage (V_{shift}).

Table 1. Simulated Gain(dB)/Phase margin(°)/Gain Bandwidth(MHz) resulting for a stress time of 10 Yrs.

	V_{DD} (V)					
Temp (°C)	1			1.1		
25	59.81	88.98	736.52	59.79	88.96	736.27
85	59.79	89	736.56	59.72	88.84	736.52

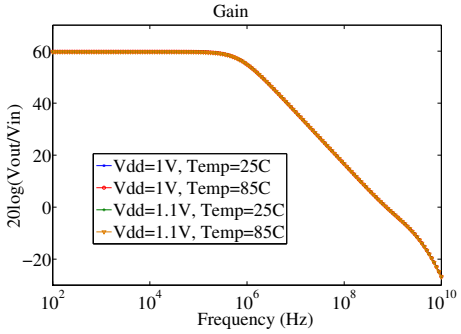

Fig. 5. Simulated Gain (dB) resulting in the buffer circuit for a stress time of 10 Yrs.

4 Aging simulation results

OTA performances at nominal condition (before stress, Temp = 25°C and $V_{DD} = 1$ V) are listed below. Here V_{offset} refers to output referred offset.

$$\text{DC Gain} = 59.71\,\text{dB} \quad \text{Gain Bandwidth} = 736.8\,\text{MHz}$$
$$\text{Phase Margin} = 89° \quad V_{\text{offset}} = 0\,\text{V}$$

The aging simulations were performed using AC input signals of $a_{\text{inp}} = 0.6V_{p-p}$, 1.1MHz sine wave, and $a_{\text{inn}} = 0.6V_{p-p}$, 1.1 MHz, 180° phase shifted sine wave. The bias voltages are $V_{\text{refp}} = 0.8$ V, $V_{\text{refn}} = 0.2$ V, $V_{\text{cm}} = 0.5$ V, $V_{\text{shift}} = 0.8$ V, Clk = 20 MHz). Figure 5 illustrates the gain Bode plot for the OTA at different V_{DD} and Temp stress conditions, simulated for stress time (Age) of 10 years. In the OTA circuit, mainly the bias current through transistors N_3 and N_{10} decides the gain, phase margin and bandwidth. These transistors see only limited gate and drain voltages, so no remarkable degradation occurs. Consequently, it can be observed from Fig. 5 and the results given in Table 1 that no significant performance degradation of these parameters (less than 1%) was observed after aging since this bias current is not affected. This shows that the current mirror structures are robust towards aging effects.

The spectral behavior of the buffer circuit was studied to see if any significant non-linearity is introduced due to circuit aging. The simulation results are depicted in Figs. 6 and 7. There is no significant difference in the spectral performances before and after aging.

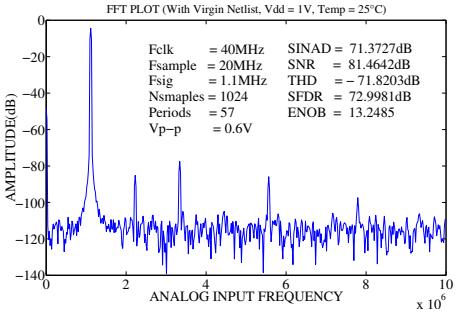

Fig. 6. FFT Spectrum results from fresh netlist.

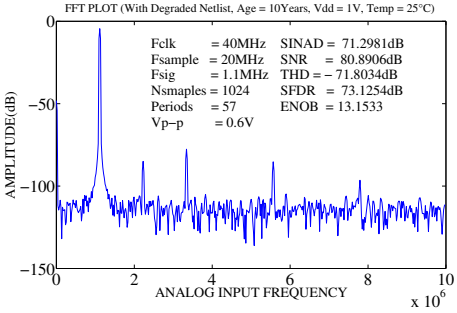

Fig. 7. FFT Spectrum results from degraded netlist.

However in closed loop configuration aging degradation leads to considerable V_{offset} in the differential output pair due to the asymmetry of the stress conditions on these two transistors: P5 is connected to $V_{\text{out}}+$ and sees high positive voltages, whereas P4 sees much lower voltages at $V_{\text{out}}-$. Table 2 summarizes the degradation-induced output referred V_{offset} simulated at different V_{DD} and Temp stress conditions for an age of 10 years. The corresponding input referred offset is obtained by dividing these values with the gain of the OTA, and it is found to be quite small due to a large gain.

5 Impact of aging on circuit performance

To study more closely the particular contribution of each transistor in the buffer circuit to V_{offset}, we evaluate its sensitivity towards V_{th} and I_d shift resulting from circuit aging. V_{offset} is calculated in this sensitivity analysis based analytical evaluation (More et al., 2010) using Eq. (5). For each transistor (T_n), the sensitivity ($S_{V_{Tn}}$) of V_{offset} towards V_{th} shift as well the sensitivity ($S_{I_{Tn}}$) towards I_d shift is determined by circuit simulation and is then multiplied with the respective V_{th} and I_d shifts. Finally, the total offset voltage shift is summed up. The results of this analysis are matching closely with results obtained by circuit simulation using RelXpert, as illustrated in Table. 2.

$$V_{\text{offset}} = S_{V_{T1}} \cdot Vt_{\text{shift}_{T1}} + S_{V_{T2}} \cdot Vt_{\text{shift}_{T2}} + \ldots + S_{I_{T1}} \cdot Id_{\text{shift}_{T1}} + S_{I_{T2}} \cdot Id_{\text{shift}_{T2}} + \ldots \quad (5)$$

Table 2. Output referred V_{offset} in (mV) resulting in the buffer circuit for a stress time of 10 Yrs.

Temp (°C)↓	Simulated	Sens. Analysis
$V_{DD} \rightarrow$	1/1.1	1/1.1
25	−1.357/8.446	−1.33/8.48
85	6.722/18.086	6.735/18.185

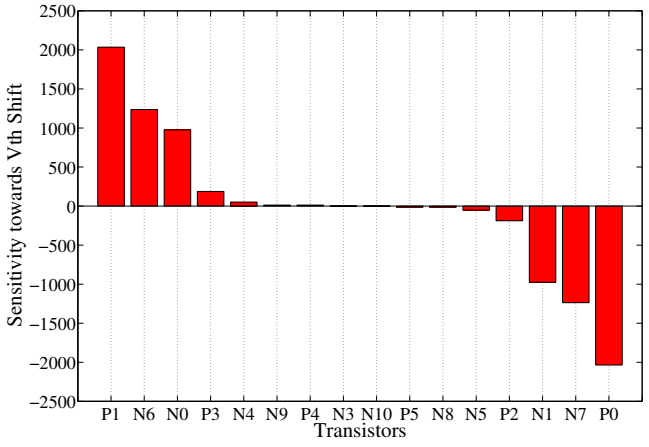

Fig. 8. Sensitivity of V_{offset} towards V_{th} shift of different transistors in the OTA circuit.

The sensitivity of V_{offset} towards V_{th} and I_d shift of all transistors in the buffer circuit is illustrated in Figs. 8 and 9.

The data in Figs. 10 and 11 represents V_{th} and I_d shift respectively, in different transistors of the OTA circuit resulting due to aging. The V_{th} shift is a combined effect of BTI and HCI and I_d shift is a combined effect of HCI and NCHCI degradation.

In Figs. 12 and 13 the contributions to V_{offset} due to aging of the individual transistors are given. These are the theoretical intermediate results obtained by multiplying the V_{th} and I_d shift for each transistor with respective sensitivity of V_{offset}. The NBTI degradations of the pMOS transistors P_0 and P_1 in Fig. 12 are of equal magnitude and compensate each other in their effect on the offset, since they see the same gate to source voltage coming from the common mode (cm) feedback circuit. Thus their NBTI degradation causes negligible V_{offset} change. The same holds true for transistors P_2 and P_3. As mentioned before, the dominant contribution to V_{offset} due to V_{th} shift comes from the pMOS transistors of the output stage, P_4 resulting from HCI (50.56%) and NBTI (49.44%) followed by P_5 resulting from HCI (38.87%) and NBTI (61.13%). Although the sensitivity of V_{offset} towards V_{th} shift of transistors P_4 and P_5 is low (±12.67) the difference between their V_{th} shifts leads to a significant impact on V_{offset}.

Figure 13 shows that the dominant contribution to V_{offset} due to I_d shift comes from pMOS transistors P_4 and P_5 resulting from HCI degradation. Although the sensitivity of V_{offset} towards I_d shift of transistors P_4 and P_5 is low (±1.09) the difference between their I_d shift leads to a significant impact on V_{offset}. The effects of transistors P_2 and P_3 again cancel each other. Comparison of Figs. 12 and 13 shows that V_{th} shift is the dominant contribution (85.9%) to V_{offset} compared to I_d shift (14.1%).

In summary, the degradation due to circuit aging affects almost all transistors in the buffer circuit. The most degraded circuit performance is V_{offset}. Since the OTA in the buffer circuit always operates in closed loop configuration, its input transistors see smaller stress compared to the output stage transistors. Simulation results show that these output transistors are the main contributors to V_{offset}. The results presented here are in-line with experimental findings from (Chouard et al., 2010b).

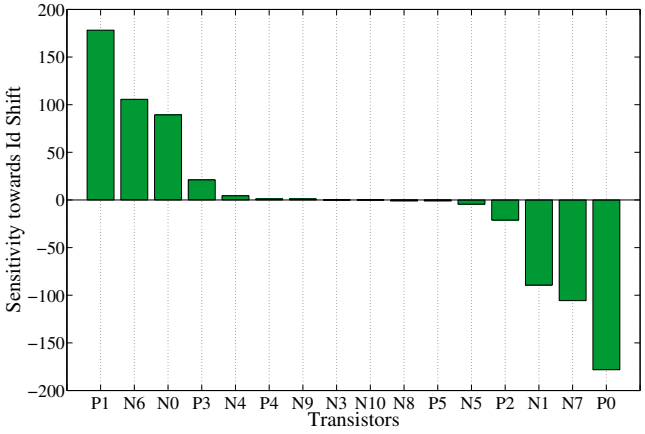

Fig. 9. Sensitivity of V_{offset} towards I_d shift of different transistors in the OTA circuit.

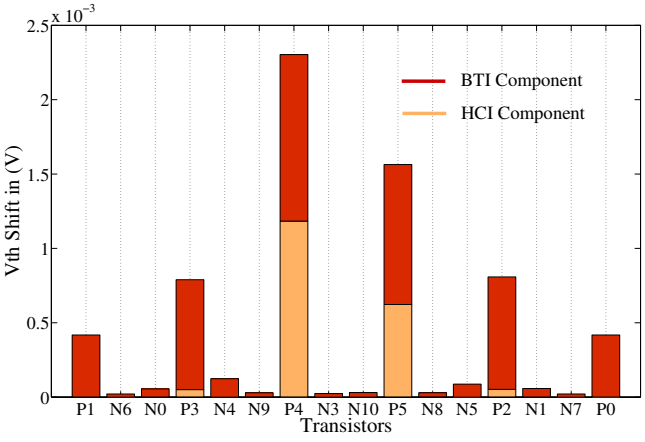

Fig. 10. NBTI, PBTI and HCI degradation component in V_{th} shift simulated for stress time of 10Yrs at $V_{DD} = 1$ V and Temp = 85 °C.

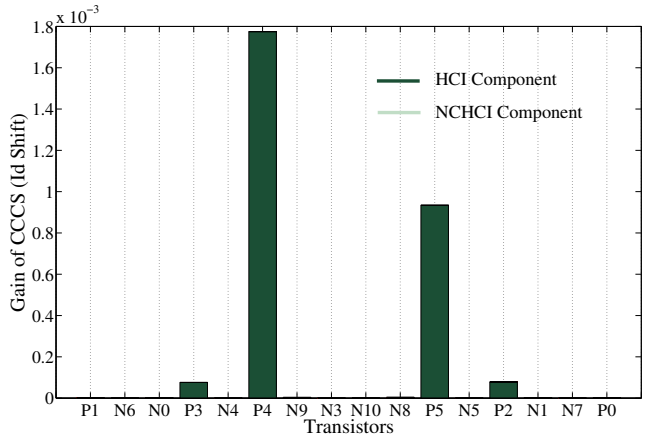

Fig. 11. HCI and NCHCI degradation component in I_d shift simulated for stress time of 1 Yrs at $V_{DD} = 1$ V and Temp = 85 °C.

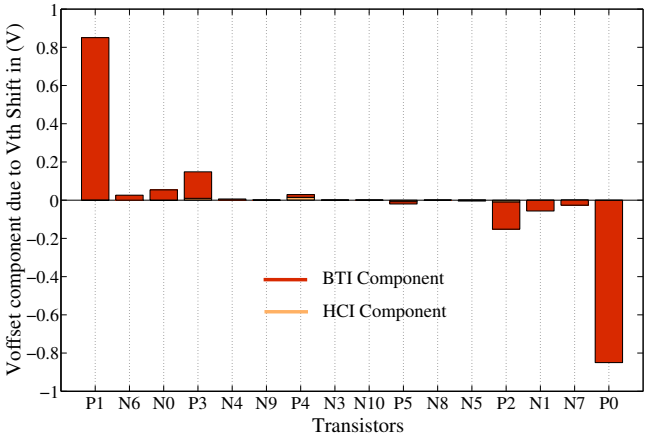

Fig. 12. Contribution to V_{offset} due to V_{th} shift resulting from NBTI, PBTI and HCI degradation, simulated for stress time of 10 Yrs at $V_{DD} = 1$ V and Temp = 85 °C.

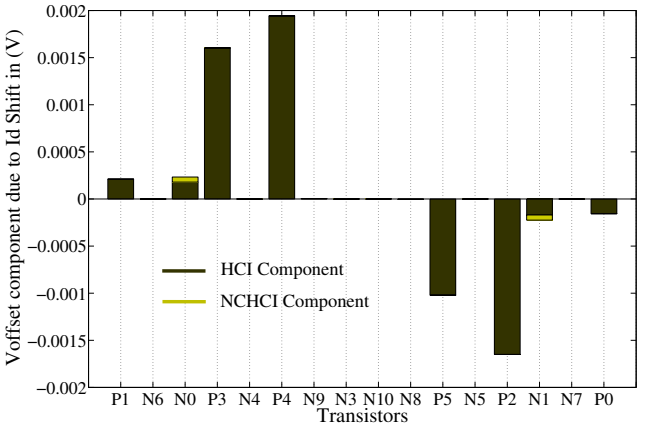

Fig. 13. Contribution to V_{offset} due to I_d shift resulting from HCI and NCHCI degradation, simulated for stress time of 10Yrs at $V_{DD} = 1$ V and Temp = 85 °C.

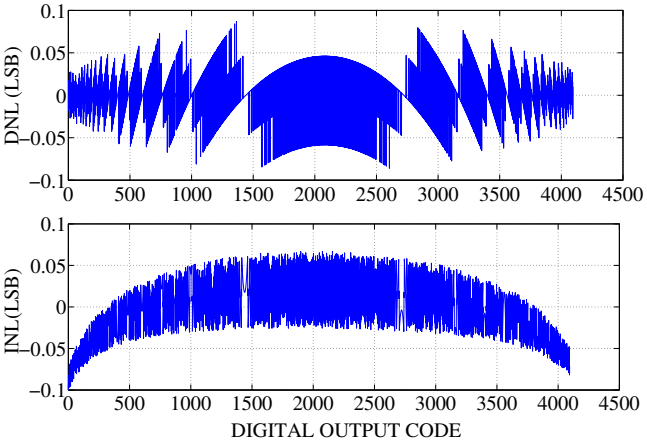

Fig. 14. Simulated DNL and INL of ADC with 10mV input referred offset in the buffer circuit.

6 Impact on ADC performance

To study the impact of an aged buffer circuit on the performance of a successive approximation ADC circuit, a 12 bit SAR ADC with charge redistribution as illustrated in Fig. 3 was modeled. All the circuit blocks were modeled as ideal elements using Verilog-A to reduce the complexity and the simulation time. A stress induced input referred offset as high as 5mV has been reported for an OTA circuit operated in closed loop configuration (Chouard et al., 2010b). So an input referred offset of 10 mV was assumed as worst case condition for the simulations. The converter was simulated with a clock frequency of 33.33 MHz, and a conversion rate of 1.19 MS/s was used with $V_{\text{refp}} = 0.8$ V, $V_{\text{refn}} = 0.2$ V and $V_{DD} = 1$ V.

The simulated differential non-linearity (DNL) and integral non-linearity (INL) are shown in Fig. 14. The resultant ENOB is 11.98 bits, which shows that the linearity of this SAR ADC is not affected by the aged buffer circuit. It was confirmed by simulations that also the spectral characteristics of the ADC were not affected. However, the transfer characteristics depicted in Fig. 15 shows that a gain error arises in the converter. All SAR ADC's having resolution (1 LSB) value smaller than the worst case input referred offset will be affected by aging degradation in this manner, with magnitude depending on the offset. There are proven methods to correct a gain error. But it is important to note that this error will vary over time. Hence special countermeasures need to be implemented to guarantee a stable and correct circuit function for the whole lifetime of the circuit.

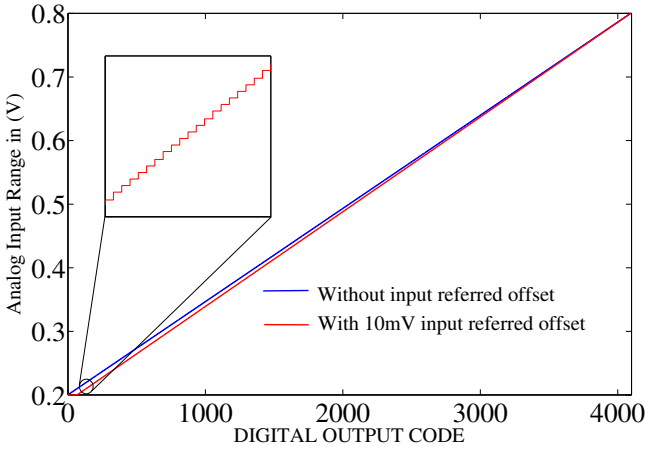

Fig. 15. Simulated input vs. output characteristics of ADC with (10 mV) and without input referred offset in the buffer circuit.

7 Conclusions

In this paper a buffer circuit designed in a 32 nm high-k, metal gate technology was analyzed by simulation for reliability with device aging. It was found that the most severely affected performance due to aging is amplifier offset, which leads to time varying gain error in an ADC circuit. Comparing Bode plots and spectal characteristics of the buffer circuit before and after aging, it could be observed that the amplifier gain, bandwidth, phase margin and spectral performance are not degraded due to aging. In a successive approximation ADC, the main effect due to aging is a time varying gain error. This leads to the conclusion that there is a need to implement special countermeasures in ADCs which correct for time varying errors resulting from stress induced degradation.

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References

Chouard, F., Fulde, M., and Schmitt-Landsiedel, D.: Reliability Assessment of Voltage Controlled Oscillators in 32nm High-k Metal Gate Technology, in: European Solid-State Circuits Conference, ESSCIRC Proceedings, 410–413, 2010a.

Chouard, F., Fulde, M., Werner, C., and Schmitt-Landsiedel, D.: A test concept for circuit level aging demonstrated by a differential amplifier, in: IEEE International Reliability Physics Symposium, IRPS, 826–829, 2010b.

Fulde, M., Schmitt-Landsiedel, D., and Knoblinger, G.: Analog and RF design issues in high-k and multi-gate CMOS technologies, in: IEEE International Electron Devices Meeting, IEDM, p. 447, 2009.

Grasser, T., Kaczer, B., Hehenberger, P., Gos, W., O'Connor, R., Reisinger, H., Gustin, W., and Schlunder, C.: Simultaneous Extraction of Recoverable and Permanent Components Contributing to Bias-Temperature Instability, in: IEEE International Electron Devices Meeting, IEDM, 801–804, 2007.

Huard, V., Parthasarathy, C., Bravaix, A., Guerin, C., and Pion, E.: CMOS device design-in reliability approach in advanced nodes, in: IEEE International Reliability Physics Symposium, 624–633, 2009.

Jha, N., Reddy, P., Sharma, D., and Rao, V.: NBTI degradation and its impact for analog circuit reliability, IEEE Transactions on Electron Devices, 52, 2609–2615, 2005.

Kaczer, B., Grasser, T., Martin-Martinez, J., Simoen, E., Aoulaiche, M., Roussel, P., and Groeseneken, G.: NBTI from the perspective of defect states with widely distributed time scales, in: IEEE Internationa lReliability Physics Symposium, 55 –60, 2009.

Martin-Martinez, J., Rodriguez, R., Nafria, M., and Aymerich, X.: Time-Dependent Variability Related to BTI Effects in MOSFETs: Impact on CMOS Differential Amplifiers, IEEE Transactions on Device and Materials Reliability, 9, 305–310, 2009.

More, S., Fulde, M., Chouard, F., and Schmitt-Landsiedel, D.: Sensitivity Analysis Based Analytical Evaluation of Aging Degradation in Linear Circuits, in: European Solid-State Circuits Conference Fringe Session, ESSCIRC, 2010.

RelXpert, C.: Users Manuals BSIMPro+/RelXpert/UltraSim, Cadence Design Systems Inc, 2010.

X. Chen et al.: A cost effective 32nm high-K metal gate CMOS technology for low power applications with single-metal gate-first process, in: Symposium on VLSI Technology, 88–89, 2008.