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Pushing energy savings in adiabatic logic by carbon-nanotube field effect transistors

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Abstract. For the first time carbon nanotube (CNT) transistor based adiabatic logic (AL) was analyzed in this work and compared to CNT based static CMOS (CCNT). Static CCNT inverters are used as a reference and compared to inverters in the AL families Efficient Charge Recovery Logic (ECRL) and Positive Feedback Adiabatic Logic (PFAL) in terms of energy dissipation. Energy savings by adiabatic logic in dependence of operating frequency, supply voltage and number of nanotubes per transistor are reviewed. It is shown that CNT based AL circuits provide high energy saving factors even for high frequencies compared to CNT based static CMOS circuits.

1 Motivation

Aggressive scaling of bulk MOSFETs has led to problems occurring due to increased short-channel-effects (SCE), leakage currents, and also due to fabrication limitations. One potential future replacement for bulk MOSFETs is the so-called Carbon Nanotube (CNT) FET. Made out of a wrapped around single-atom thick carbon cylinder, they promise to have excellent electrical as well as mechanical behavior. CNTs can be metallic or semiconductors (small-gap or moderate-gap), depending on the way they are rolled and the circumference of the tube (Hamada et al., 1992). So both, active devices and connections can be made out of CNTs. Single Wall Carbon Nanotubes (SWCNT) have a high mobility in the order of $100\,000\,\mathrm{cm^{-2}\,Vs^{-1}}$ and a conductivity of up to $400\,000\,\mathrm{S\,cm^{-1}}$ (Hecht, 2007), due to the 1-D transport and thus reduced phase space for scattering leading to ballistic transport (Javey and Dai, 2006). Though these facts are very convincing, a lot of barriers have to be overcome before MOSFETs made out of SWCNTs can be produced on a large scale. One limitation is the Schottky Barrier (SB) that is formed by any metal-semiconductor connection due to the different work functions (Appenzeller et al., 2002). This limits the on-state current and thus the performance of the device. Additionally this leads to an ambipolar characteristic (Martel et al., 2001), the on-current is increased, when $|V_{\mathrm{GS}}|$ is increased. In digital circuits, this leads to problems in transistor stacks, where negative gate-to-source voltages appear and thus turn on a device that has a "0" input (Raychowdhury and Roy, 2007). One way to overcome this limitation is by connecting the nanotubes via Palladium, which is a metal with a high work-function (Javey et al., 2003). Thus the barrier can be greatly reduced or eliminated. Chirality cannot be controlled so far, nanotubes are to date a mix of 1/3 metallic and 2/3 semiconducting tubes (Hecht, 2007). The controlled assembly of nanotubes is another barrier that has to be overcome in order to allow for the integration of systems consisting of CNT devices with traditional metal interconnects, or CNT only. Derycke et al. (2001) propose a methodology to selectively produce p-type and n-type CNTs for inter-nanotube inverters. One of the tubes is covered with Polymethylmethacrylat (PMMA) and after thermal annealing and following exposure to oxygen, one of the tubes is n-type and the other is a p-type tube.

In contrast to dynamic losses in static CMOS

$$E_{\mathrm{CMOS}} = \frac{1}{2} \cdot C \cdot V_{\mathrm{DD}}^2 \tag{1}$$

the losses in adiabatic logic (AL) are described by

$$E_{\mathrm{AL}} = 8 \cdot \frac{RC}{T} \cdot C \cdot V_{\mathrm{DD}}^2 \tag{2}$$

The losses in AL do not only depend on the capacitance C and the voltage supply V_{DD} but also on the path resistance R and the period T of the operating frequency.

Due to their superior electrical characteristic, the high conductivity resulting from a (near-)ballistic transport, carbon nanotubes are interesting candidates for future large scale integration circuits; their capabilities allow for lowest consumption especially in Adiabatic Logic. In the following part of the work the principle of chirality and its meaning

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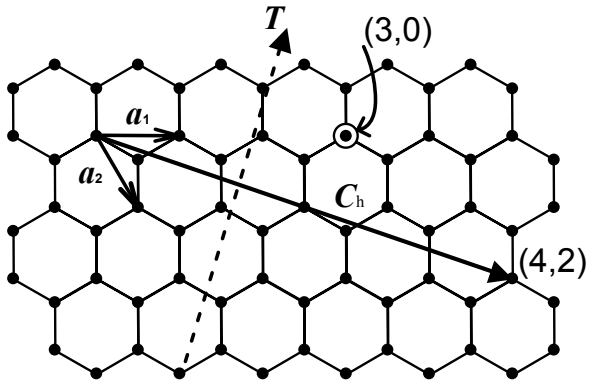

Fig. 1. The chiral vector $\boldsymbol{C}_\mathrm{h}$ is defined via unit vectors $\boldsymbol{a}_1$ and $\boldsymbol{a}_2$. It defines the electrical properties. As examples, the metallic $(3,0)$ and a semiconducting $(4,2)$ orientation is presented. Perpendicular to the chiral vector the translation vector $\boldsymbol{T}$ is found, which is the axis of the obtained nanotube.

for the properties of CNTs will briefly be presented, and later on, simulations are carried out with the Stanford CNT Hspice simulation model (Deng et al., 2008; Deng and Wong, 2007a,b) to see how Adiabatic Logic performs with those future devices.

2 The chirality of a CNT and the CNTFET

A CNT can be either metallic or semiconducting. The chiral vector $\boldsymbol{C}_\mathrm{h} = n_1\boldsymbol{a}_1 + n_2\boldsymbol{a}_2$ determines whether a metallic or semiconducting nanotube is formed. A graphical representation of the chirality vector can be observed in Fig. 1. It connects the origin with the point on the grid that is identical to the origin after wrapping up the carbon sheet. With the chiral number (n_1,n_2) the circumference of the nanotube can be determined as $|\boldsymbol{C}_\mathrm{h}| = a\sqrt{n_1^2+n_2^2+n_1n_2}$, where $a = 2.49$ Å is the bond distance of two carbon atoms. Electrical characteristics are also determined via the chiral number. A nanotube with (n_1,n_2) is a metal, if $n_1 - n_2 = 3l$ $(l = 1,2,3\ldots)$ and a semiconductor if $n_1 - n_2 \neq 3l$ (Dresselhaus et al., 2001). The bandgap energy E_gap is also dependent on the circumference of the tube. Additionally, tiny-gap and large-gap semiconducting CNT exists, also deterministic according to the chiral number (n_1,n_2) (Hamada et al., 1992). Two constellations are pictured in Fig. 1, the chiral number $(3,0)$ represents a metallic nanotube, whereas the $(4,2)$ constellation is a semiconducting nanotube. For tiny-gap and large-gap semiconducting CNTs the bandgap energy is proportional to $\frac{1}{R^2}$ and $\frac{1}{R}$, respectively (Dresselhaus et al., 2001), where R is the radius of the tube.

Figure 2 shows a schematic cross-section through a CNTFET device. The source and drain regions are connected by a semiconducting CNT. As in the bulk MOSFET device, the control gate of the CNTFET is separated from the semiconductor with an insulating layer.

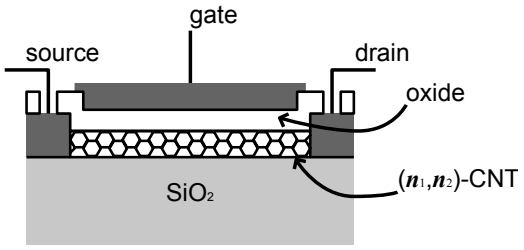

Fig. 2. Schematic cross-section of a Carbon Nanotube Field Effect Transistor (CNTFET) proposed by Marulanda (2008). A gate is separated via an insulating layer (oxide) from the CNT. Through the CNT a connecting channel between source and drain can be established.

Table 1. Parameter list for the applied Stanford CNT simulation model.

Parameter	Value	Explanation
V_DD	1.2 V	supply voltage
(n_1,n_2)	$(19,0)$	chirality of nanotube(s)
tubes	3	# of parallel tubes within a device
pitch	20 nm	distance between adjacent CNTs
L_ch	32 nm	physical channel length
$L_\mathrm{SS}, L_\mathrm{DD}$	32 nm	doped source/drain extension
t_ox	4 nm	top gate oxide thickness
k_ox	16	dielectric constant of oxide

3 Simulation results

Simulations are carried out with the HSpice CNT compact model provided by Deng and Wong (2007a,b) and Deng et al. (2008). The model includes non-idealities like near-ballistic transport, scattering, effects of the source/drain extension, and charge screening between tubes, when more than one tube is used for a CNTFET (Deng and Wong, 2007a). By inclusion of a transcapacitance network, good predictions of the transient behavior are expected (Deng and Wong, 2007a).

Based on the Stanford CNT model, static CMOS like (static CCNT) inverters as well as adiabatic inverters are compared with respect to the energy consumed per performed calculation. The standard parameter sets summarized in Table 1 are used if not stated otherwise. Three tubes in parallel are used in the CNTFET devices, each with a moderate-gap semiconductor tube of chiral number $(19,0)$. Pitches between the adjacent CNTs within one device are 20 nm. A channel of 32 nm physical length is separated via a 4 nm oxide. A chain of five inverters is used to determine the energy consumption and therewith the resulting energy saving factor ESF$= \frac{E_\mathrm{CMOS}}{E_\mathrm{AL}}$. The static CCNT structure is used as

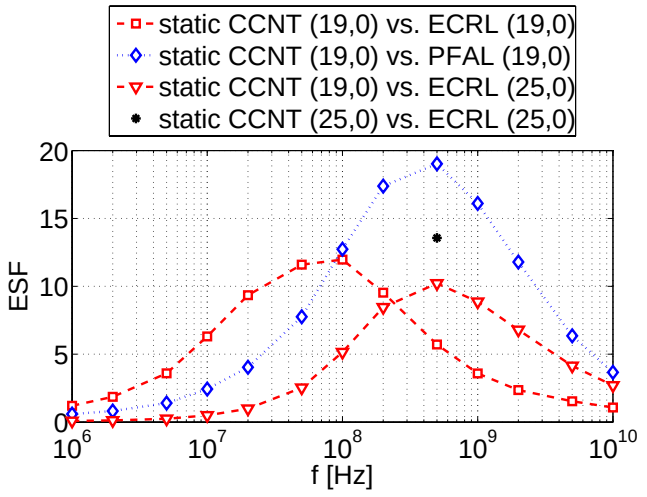

Fig. 3. The ESF gained by applying CNTFETs for ECRL and PFAL.

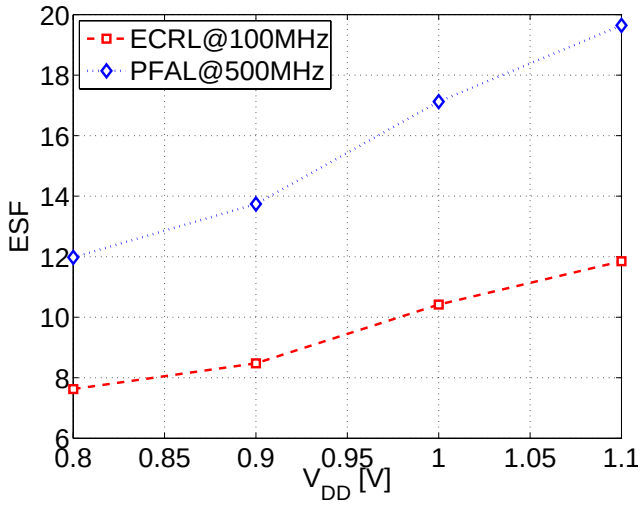

Fig. 4. Development of the ESF of an inverter circuit under the impact of voltage scaling.

a reference and compared to inverters in the AL families Efficient Charge Recovery Logic (ECRL, Moon and Jeong, 1996) and Positive Feedback Adiabatic Logic (PFAL, Blotti et al. 2000).

ESF versus the frequency can be observed in Fig. 3. A maximum ESF of 12 is found for ECRL for 100 MHz and 19 for PFAL at 500 MHz. A remarkable result is, that for a wide frequency range from 70 MHz to 2.4 GHz the ESF is above 10 for PFAL. If the chiral vector is changed, the bandgap of the semiconductor is influenced. A reduced bandgap energy leads to a reduced threshold-voltage V_{th}, as the barrier height from source/drain to the channel is reduced. The on-current is increased, but off-currents are also increased. Due to the reduced V_{th} leakage currents are increased, but the adiabatic losses are reduced, as the gate-overdrive $(V_{\mathrm{DD}} - V_{\mathrm{th}})$ is increased. ECRL is simulated for $(25,0)$ and compared to static CCNT $(19,0)$. For the frequency with maximum ESF also the static CCNT with $(25,0)$ is simulated and compared to ECRL $(25,0)$. For lower frequencies, increased leakage currents lead to an intersection of leakage losses and adiabatic losses for the $(25,0)$ ECRL configuration, i.e. leakage dominates the losses. That leads to decreased ESF when compared to the case of $(19,0)$ chirality. Reduced adiabatic losses lead to a shift of the optimum frequency f_{opt} (frequency with maximum ESF) to 500 MHz. At this frequency the ESF for $(25,0)$ is higher compared to its $(19,0)$ counterpart. Thus f_{opt} can be adopted by changing the chirality of the nanotube. At 500 MHz the static CCNT inverter was simulated with $(25,0)$. An increase in the ESF is observed, that can be explained by increased leakage currents in the $(25,0)$ static CCNT. For static CCNT circuits, performance is improved but dynamic losses are not directly impacted by the chirality.

In summary, the following values are derived from Fig. 3: f_{opt} is improved from 100 MHz to 500 MHz and the maximum ESF is decreased from 12 to 10 in case of replacing $(19,0)$-tubes in ECRL with $(25,0)$-tubes, and it is increased from 12 to 13.6 in case that $(25,0)$-tubes are used both in ECRL and static CCNT.

PFAL for the $(19,0)$-setup has already a high ESF with a maximum value of 19 at 500 MHz. Increasing the chirality for PFAL to $(25,0)$ did not show any benefit, it rather worsens the energy behavior of PFAL. Thus it is not presented in the figures.

All previous investigations are carried out with a supply voltage of $V_{\mathrm{DD}} = 1.2$ V. Supply voltage scaling allows to reduce the energy dissipation in static CCNT and AL. Simulations are carried out with reduced supply voltage. The according ESFs are presented in Fig. 4. It is reduced by 34% and 39% when going from 1.1 V to 0.8 V for ECRL and PFAL, respectively. But it has to be mentioned, that the performance for static CCNT is also decreased. As cascaded gates are used, the overall performance loss will decrease the maximum operating frequency or the effort for pipelining is increased. The first fact will determine a lower limit for voltage scaling (where safety margins for variations have to be regarded also), whereas the second fact leads to a trading of speed versus energy and area.

A high fan-out of a gate leads to the necessity of scaling the devices of the driving gate. Comparable to the width in planar CMOS technology, the number of tubes is a measure in CNTFETs for their driving capability. Equipping a gate with a higher number of tubes in the devices will impact the energy dissipation. Figure 5 shows the simulation results of ESF, when different numbers of tubes are used within the inverter chain. All gates in the chain are sized, and both devices, NCNT and PCNT. Again ECRL and static CCNT

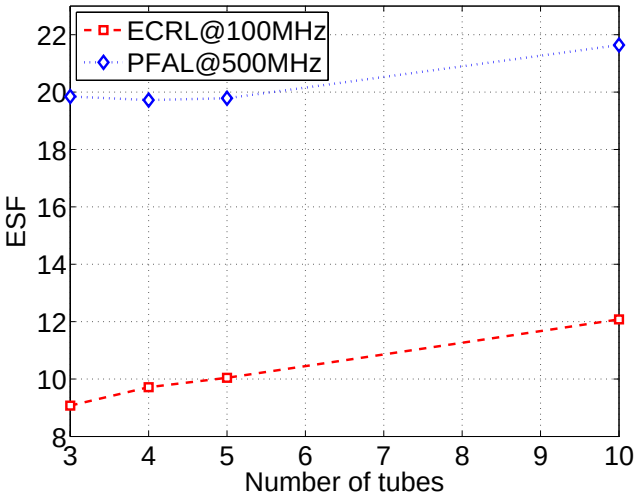

Fig. 5. ESF with respect to the number of parallel tubes used in a CNTFET device.

are simulated with a frequency of 100 MHz, and PFAL at 500 MHz, all with a supply voltage $V_{DD} = 1.2$ V. The increased number of tubes obviously impacts the ESF. While the ESF for PFAL stays constant up to five tubes in parallel, and is increased from 20 to 22 when ten tubes are used, in ECRL it is continuously increased from 9 for three tubes to 12 in case of ten tubes. This is explained by the increased capacitance value and the reduced on-resistance due to parallel connection of more tubes. In static CMOS, the increased capacitance will increase the energy dissipation according to $E_{CMOS} \propto C$. In AL, also the reduced on-resistance impacts the energy dissipation with $E_{AL} \propto RC^2$. If the quadratic increase of the capacitance value is more than compensated by the reduced on-resistance, the energy in AL rises less than in static CCNT.

4 Summary and conclusions

For the first time carbon nanotube based adiabatic logic was analyzed in this work and compared to CNT based static CMOS. Simulation results show maximum energy saving factors of 12 and 19 for ECRL and PFAL, respectively. A remarkable result is, that for a wide frequency range from 70 MHz to 2.4 GHz the ESF is above 10 for PFAL. Changing the chirality to $(25,0)$ will impact results for ECRL: ESF factors for frequencies greater than 100 MHz are increased with respect to the $(19,0)$ results. The optimum frequency is increased from 100 to 500 MHz. The maximum ESF is slightly decreased. If carbon nanotubes become successors to planar CMOS transistors they offer a tremendous energy saving impact and improved performance especially in Adiabatic Logic. Due to their superior carrier transport they offer a small on-resistance and thus are exceptionally well applicable in Adiabatic Logic, where energy per operation depends not only on capacitance, as in static CMOS, but also on on-resistance.

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