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Circuit design with adjustable threshold using the independently controlled double gate feature of the Vertical Slit Field Effect Transistor (VESFET)

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Abstract. The recently introduced Vertical Slit Field Effect Transistor allows for adjusting its threshold voltage through independent controllable gates. This feature can be applied to a broad range of circuits. In this paper two examples are presented. First, a ring oscillator with a wide frequency tuning range and second, a Schmitt trigger with a controllable hysteresis.

1 Introduction

The **VE**rtical **S**lit **F**ield **E**ffect **T**ransistor (VESFET) is a novel transistor concept, which comes along with a new manufacturing and design paradigm, and is based on the ideas and vision of Wojciech Maly (Maly, 2007). The key concept of this paradigm is the use of identical unit sized devices, which are placed in a highly regular manner together with highly regular interconnects (Maly et al., 2007; Lin et al., 2009). This approach of ultimate regularity may allow for cost efficient manufacturing as the key objective of the VESFET technology (Maly and Pfitzner, 2008). At the same time the design flexibility is maintained and with the inherent properties of the VESFET, one can create circuit innovations.

One key leverage of the VESFET is that the gates can be controlled independently. This feature allows to implement additional logic functionality into one transistor using an AND- and OR-VESFET (Weis et al., 2009a,b). The independent gate control is not limited to logic circuits and can be used also for SRAM memory cells to increase the performance (Weis et al., 2008).

This paper extends the use of the independent double gate feature of VESFET. In the subsequent Sect. 2, the structure, the working principle, and the independent double gate operation of the VESFET are introduced. In Sect. 3, circuit examples are discussed using the adjustable threshold of the VESFET for tunable ring oscillators and a Schmitt trigger circuit.

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2 Vertical Slit Field Effect Transistor (VESFET)

The VESFET is a four terminal device with source, drain and two gates. The square shaped unit device is built on silicon-on-insulator and all devices are separated to each other. The four terminals are constructed by vertical metal pillars with a radius r. The radius r defines the width of the vertical slit $w_s = r(\sqrt{8}-2)$ and the footprint of the whole device with a total area of $64r^2$. One possible implementation of the VESFET is shown in Fig. 1 for the top view and a bird's eye view, which exhibits the height h of the VESFET structure. The channel volume is defined by the distance between the source and drain terminal as well as the height h and the width of the vertical slit between the two gates.

2.1 Working principle

The VESFET is a pn-junction-less transistor with a gate controlled bulk current, using either a p- or n-type substrate for the complementary transistor types. It can be regarded as a hybrid of a Junction Field Effect Transistor (JFET) and a MOSFET. The operation is JFET-like because it is based on transport of majority carriers in a bulk channel, whose effective width is controlled by depleted regions induced by two gates on both sides of this channel. The gates, however, are separated from the channel by an insulating layer, like in a MOSFET. The difference to the MOSFET is that the current is not bound to an inversion channel but flows through the whole bulk volume between source and drain terminal. In the off-state, the depletion regions induced by the two gates fill the whole channel and the device is non-conducting. For a normally "OFF" transistor the gate material has to be chosen

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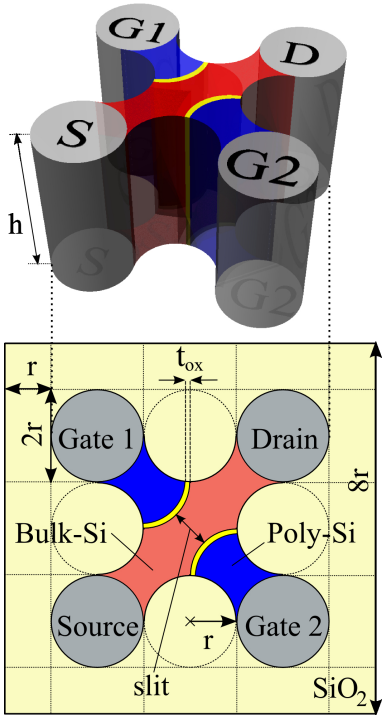

Fig. 1. Vertical **S**lit **F**ield **E**ffect **T**ransistor (VESFET).

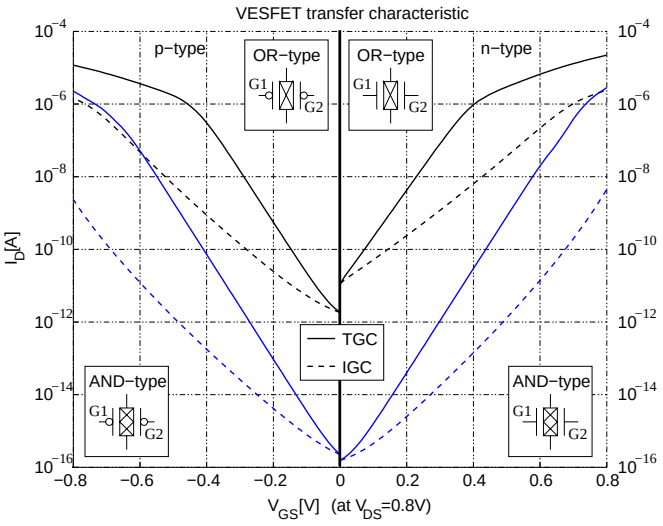

Fig. 2. VESFET transfer characteristics and transistor symbols for tied gate configuration (TGC) and independent gate configuration (IGC). VESFET parameters: $r = 50\,\text{nm}$, $h = 200\,\text{nm}$, oxide thickness 4 nm, poly-gate doping concentration $5 \times 10^{18}\,\text{cm}^{-3}$, AND-type p-substrate $1.5 \times 10^{17}\,\text{cm}^{-3}$, AND-type n-substrate p-substrate $1 \times 10^{17}\,\text{cm}^{-3}$, OR-type p-substrate $5 \times 10^{17}\,\text{cm}^{-3}$, OR-type n-substrate p-substrate $4 \times 10^{17}\,\text{cm}^{-3}$.

such that for an n-type transistor and the gates biased "low", the depletion widths are close to their maximum expansion, and vice versa for a p-type transistor and the gates biased "high". Applying appropriate voltages to the gates the depletion regions withdraw and a conducting path from drain to source is established, and the transistor is in the on-state.

2.2 Independent double gate operation and adjustable threshold voltage

One key leverage of the VESFET is that the gates can be controlled independently. Consequently the threshold voltage of the VESFET is dependent on the gate-to-source voltages of the two gates. This can be used to implement a logic "OR" or "AND" functionality within one transistor. For the "OR" type transistor this means that if gate 1 is "low" and gate 2 is "high" the transistor is turned "ON" and vice versa for gate 1 is "high" and gate 2 is "low" (where "low" and "high" are the logic voltage levels). Similar for the "AND" type transistor and the gates biased in the same way as just described, the transistor is turned "OFF". For the rest of the paper this is referred to the "independent gate configuration" (IGC). For the case that both gates are "high", the transistor is turned "ON" for a n-type transistor and "OFF" for a p-type transistor and vice versa for both gates are "low". For the rest of the paper this is referred to the "tied gate configuration" (TGC), where the transistor can be treated as standard transistor with one gate only. From device simulation low power optimized transistors are derived, where Fig. 2 shows the transfer characteristic for p- and n-type for IGC and TGC and introduces the transistor symbols.

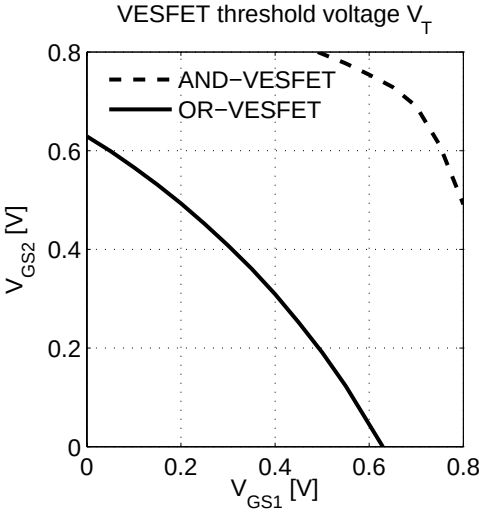

Fig. 3. n-type threshold voltage for AND- and OR-VESFET.

For the case that the potential at the gates is not limited to logic voltage levels, one can flexibly adjust the threshold voltage of the VESFET with the two gates biased independently. This behavior is shown in Fig. 3 for the just introduced AND- and OR-VESFET. The threshold voltage V_T is derived from the constant current method $V_T = V_{gs}$ at $V_{ds} = 100\,\text{mV}$ where $I_{ds} = 0.05\,\mu\text{A}$. For example, the threshold

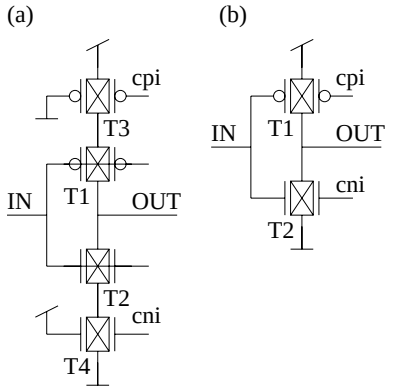

Fig. 4. Current Starved Inverters (CSI) with TGC and IGC VESFET: **(a)** four transistor implementation similar to CMOS, **(b)** two transistor implementation with the control gates merged into the inverter transistor pair.

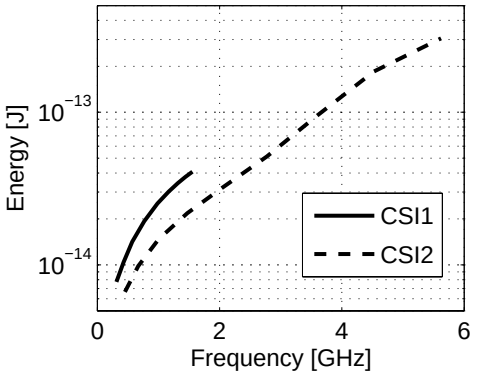

Fig. 5. Current Starved Inverter (CSI) based 11 stage tunable ring oscillators with IGC VESFET. The frequency is tuned by the control signals cpi, cni of Fig. 4.

voltage for an n-type OR-VESFET can range from $V_{gs1} = 0\,V$ to $V_{gs1} = 0.63\,V$ for appropriate biased V_{gs2}. Hence, one gate can be used to define the threshold voltage at the other gate.

3 Circuits using the adjustable threshold of the VESFET

Two possbile applications are discussed in the following to demonstrate the flexibility of the independent double gate operation of VESFET and its associated adjustable threshold voltage.

3.1 Tunable ring oscillators

One concept to build a tunable ring oscillator is the use of current starved inverters in a ring oscillator chain (Jeong et al., 1987). The idea is to control the delay of the inverters by limiting the current available to charge or discharge the output load. Two possible implementations for a current starved inverter implemented with TGC and IGC VESFET are shown in Fig. 4.

For the first implementation CSIa (see Fig. 4a) two control transistors (T3, T4) are added to the inverter pair (T1, T2). The control transistors have one gate grounded or connected to the supply voltage to guarantee a minimum current. With the second gates connected to cpi and cni, one can control the available current to charge or discharge the output load. Of course, it is also possible to use the transistors T3, and T4 in a tied gate configuration. However, the control signals cannot use the full swing between the ground and the supply voltage, because this could turn off the transistors T3 and T4 completely and the oscillation would collapse.

For the second implementation CSIb (see Fig. 4b) the control transistors are merged into the inverter. Compared to the first implementation, one can reduce the transistor count by a factor of two. Further, it allows to use the full swing for the control signals. Additionally, the transistor stack height is reduced and therefore the path resistance. As a consequence, the range to adjust the frequency is increased.

For an eleven stage ring oscillator, using the above mentioned current starved inverters, the frequency range and the dissipated energy at a supply voltage of $V_{dd} = 0.8\,V$ is shown in Fig. 5. The first implementation CSIa allows to control the frequency continuously from 0.31 to 1.55 GHz. The second implementation CSIb allows to control the frequency continuously from 0.45 to 5.62 GHz. The lower frequency bound can be achieved for the control signals at cpi$= V_{dd}$ and cni$= 0\,V$. Vice versa the upper frequency bound can be achieved for the control signals at cni$= 0\,V$ and cpi$= V_{dd}$.

One peculiarity of the second implementation is that the maximum frequency can be higher than a ring oscillator with a fixed frequency. For an eleven stage ring oscillator using TGC OR-VESFET the according frequency is 3.61 GHz. The reason is that for control signals at cni$= V_{dd}$ and cpi$= 0\,V$, the transistors T3 and T4 are always above threshold. However, the inverter inputs at the gates opposite to the controll signals will still guarantee a proper oscillation of the circuit. Of course, this leads to a higher energy consumption due to larger cross current flow from the supply rail to ground. Once the voltage range of the control signals is accordingly limited, one can avoid this increased cross current. Depending on the application requirements, this has to be considered for the circuit design.

3.2 Schmitt trigger

Another application which can benefit from an adjustable threshold is the Schmitt trigger (Schmitt, 1938). The important properties are the fast transition time due to the positive feedback and the different switching thresholds for low-to-high (LH) and high-to-low (HL) signals which form a hysteresis. Based on a CMOS implementation (Weste and Harris, 2005), a VESFET Schmitt trigger is shown in Fig. 6.

The switching thresholds are determined by the ratio of the driving strengths of the p- and n-type transistors. For the

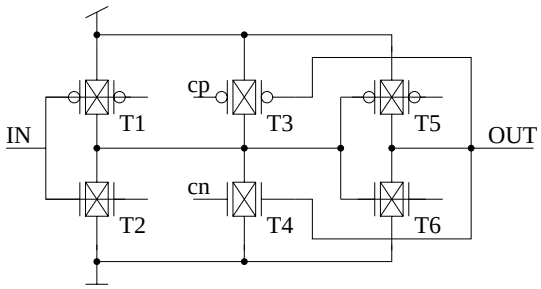

Fig. 6. Schmitt trigger with TGC and IGC VESFET. Hysteresis is controlled by cn, cp.

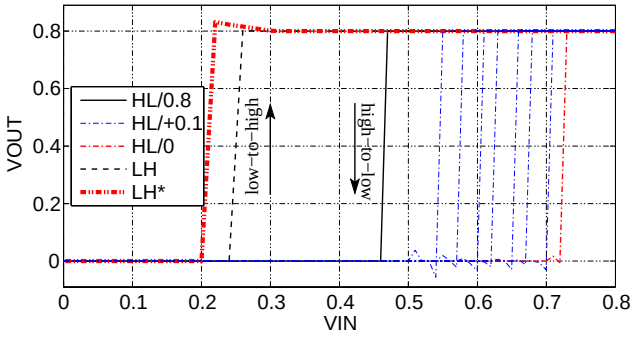

Fig. 7. Schmitt trigger hysteresis for the circuit in Fig. 6 with cn= 0 V and cp from 0 V to 0.8 V.

input and output inverting transistor pairs T1, T2 and T5, T6, OR-VESFETs are used in tied gate configuration, whereas the inverter pair T3, T4 is used in independent gate configuration, where one gate is connected to the output node and the other to one of the control signals cp, cn. With the control signals, one can change the threshold condition of the VESFET T3, T4 to adjust the hysteresis of the Schmitt trigger. The low-to-high transition can be controlled by changing the driving strength of T3. Vice versa, the high-to-low transition can be controlled by changing the driving strength of T4. The hysteresis of the output voltage V_{OUT} as a function of the input voltage V_{IN} is shown in Fig. 7. Here, the threshold voltage for the high-to-low transitions is adjusted via the control signal cp from 0 to 0.8 V in 0.1 V steps. The threshold of the low-to-high transition is kept constant using either transistor T4 in tied gate configuration (not shown) or keeping the control signal at an constant value (here cn= 0 V). For cp= 0.8 V, the high-to-low threshold (HL/0.8) is at 0.45 V, and for cp= 0 V (HL/0) at 0.73 V. The change of the threshold voltage is also shown for intermediate control voltages in steps of 0.1 V (HL/+0.1). The low-to-high threshold voltage (LH) is constant at 0.25 V for cp signals ranging from 0.8 V to 0.3 V. A further decrease of cp will also affect the low-to-high threshold voltage (LH*), because OR-VESFET T3 is always turned on. To avoid this behavior, the control voltage range should be chosen appropriately. In the same way the low-to-high transition can be adjusted by varying the control signal cn.

4 Conclusions

The independent gate configuration of VESFET is a powerful leverage for circuit design. In this paper two circuit applications are presented which can greatly benefit from the adjustable threshold voltage of the VESFET. First, it is shown that for a current starved inverter based ring oscillator a wide frequency tuning range can be achieved. Second, it is shown how the hysteresis of a Schmitt trigger circuit can be controlled. With VESFET it is possible to change the threshold voltage during operation. These benefits are not limited to the shown examples and can be further extended to a broad range of circuit applications.

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