Adv. Radio Sci., 6, 227–232, 2008
www.adv-radio-sci.net/6/227/2008/

Advances in Radio Science

Impact of on-chip inductance on power supply integrity

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Abstract. Based on product related scenarios, the impact of on-chip inductance on power supply integrity is analyzed. The impact of varying current profiles is shown to be minimal. In a regular power grid with regular bump connections, the impact of on-chip inductance on the cycle average of the supply voltage can be neglected, even for a worst case estimation of on-chip inductance. Whereas, the maximum transient power supply drop can be significantly underestimated by neglecting on-chip inductance. The impact of on-chip inductance in a System-on-Chip (SoC) environment also can be neglected if the on-chip inductance is conservativly estimated.

1 Introduction

With ongoing technology scaling, power supply integrity has become a major concern even in low power designs. Lowered supply voltages, increasing current densities, increasing operating frequencies, and increasing sheet resistances have decreased the noise margins for every process technology. This trend is expected to continue with technology scaling (Nassif and Fakhouri, 2002; Larsson, 1999; Mezhiba and Friedman, 2004). Power supply noise can be divided into two effects. The first is called IR-Drop and describes the effect of a voltage drop over the parasitic resistance of the power grid, caused by the current flowing through the grid. The second effect is called di/dt noise and describes voltage bounces caused by transient current surges over the parasitic inductance of the power grid. The parasitic inductance of the power grid can be divided into on-chip inductance, coming from all the wires on the chip, and off-chip inductance, coming from all package and board power connections. The paper will address the question, whether on-chip inductance has a significant impact on the total power supply noise bugdet. The rest of the paper is organized as follows. In Sect. 2 and Sect. 3 the movitation and the simulation setup are outlined.

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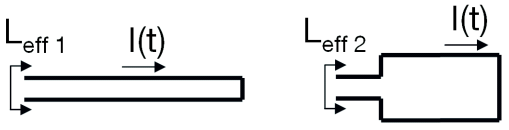

Fig. 1. Schematic of two wires with different effective inductance L_{eff}, having the same geometric dimensions

Simulation results for a worst case estimate of on-chip inductance in a regular power gird are presented in Sect. 4. An improved estimation of the effective on-chip inductance and the resulting simulation results in a SoC environment are presented in Sect. 5. Finally, the paper ends with a conclusion.

2 Motivation

As stated before, power supply noise is either caused by the parasitic resistance or the parasitic inductance of the power supply grid. The extraction of the parasitic resistance of a wire connection, or the supply grid as in our case, is straight forward. The wire is divided into several filaments, and the resistance of all the filaments is added up. The resistance extraction is state of the art and does not pose a significant challenge. However, the resulting inductance of a current loop consisting of two wire segments is given by its self and mutual inductance, as described in Eq. (1).

$$L_{\text{eff}} = L_{11} + L_{22} - 2 \cdot L_{12} \tag{1}$$

Where L_{11} and L_{22} describe the self, and L_{12} the mutual inductance of the current paths, respectively. While L_{11} and L_{22} are set by the geometric dimensions, such as width, height, and length, of the wire, L_{12} is given by the coupling and therefore by the acutal layout of the current loop. This leads to the fact, that two wires having the same geometric dimensions, width, height, and length, can have different effective inductances, as depicted in Fig. 1. Knowing this, it is obvious that the proper extraction of on-chip inductance poses a significant challenge at the design flow. Additionally, by

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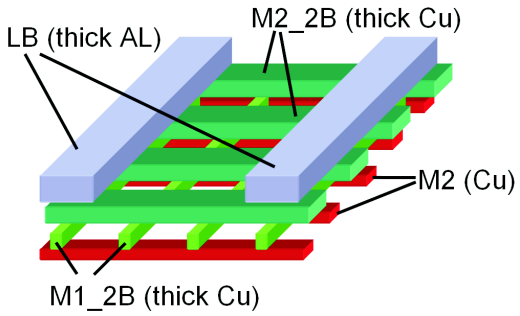

Fig. 2. Schematic of the used 4 layers power grid.

implementing distributed inductances into to the simulation setup the complexity increases significantly and increases the simulation time. Previous publications claimed that on-chip inductance has a significant impact on the design of power distribution grids (N. Srivastava, 2005). In (Mezhiba and Friedman, 2004) it was shown that the proportion of on-chip inductive noise increases with technology scaling. This paper addresses the question whether on-chip inductance has to be taken into account when analysing delay degradation due to power supply noise.

3 Simulation setup

The simulation setup considered in this analysis is similar to the setup in (Eireiner et al., 2006). As example we take a low power SoC in a 90 nm technology with an ARM926 core (Lueftner et al., 2006). The area of the entire SoC is roughly 6 mm×6 mm, the area of the ARM core is 1 mm×1 mm. The ARM core is operated at a maximum frequency f_{fast}=254 MHz and a slower frequency of f_{slow}=130 MHz. The frequency change from f_{slow} to f_{fast} is taken as exemplary di/dt noise event. During regular operation of the ARM core a peak current of $0.52A$ is assumed. The power grid consists of four metal layers, as depicted in Fig. 2, each orthogonal to its vertical neighbors, with contacts at the overlapping regions. A paired power grid structure (Mezhiba and Friedman, 2002) is used for the metal layers LB, M12B, and M22B to minimized inductive effects. The grid is modeled as a distributed R-L-C circuit built from a pi-model, as depicted in Fig. 3. The values for pi-model were choosen such that every instance of the pi-model represents a filament of the power grid 5 μm long.

As packaging technology a flipchip package is assumed. The bump connections are modeled as ideal inductances with values of $0.5nH$, $0.75nH$, or $1.0nH$ each. In Fig. 4 a schematic of a typical SoC power distribution grid is depicted. In the green region in the center of the SoC regular bump connections, depicted as grey circles, are available for power delivery. In the blue outer region no bump connections are available for power delivery due to I/O and ESD restrictions. In our analysis two different grid scenarios, which can occur in a SoC design, are analysed. The first is called "regular grid". It describes the case in which the on-chip power grid is connected to the package with regular bump connections, as depicted in Fig. 5. As second case, a so called "SoC grid" is analysed. In this scenario cores are placed at least partly in the outer region, where no bump connections can be used for power delivery, see Fig. 4. The coloured rectangles in Fig. 4 represent three exemplary positions of the ARM core, "lower left", "middle", and "center" for the yellow, orange, and blue rectangle, respectively. The dashed purple rectangle in Fig. 4 and Fig. 5 indicate the same area. For inductance extraction the tool FastHenry was used (Kamon et al., 1994). With FastHenry the self inductance and the mutual inductances of all parts of a current loop and the resulting effective inductance are determined. As shown in (Saint-Laurent and Swaminathan, 2004) and verified in (Eireiner et al., 2006), the cycle average of the supply voltage determines the delay of logic circuits. Therefore, the cycle average of the supply voltage, V_{supply}, is taken as key metric for delay degradations, where V_{supply} is defined as the difference between V_{DD} and V_{SS}, $V_{\text{supply}}=V_{DD}-V_{SS}$. As mentioned

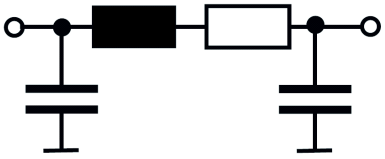

Fig. 3. Schematic of a single R-L-C pi-model.

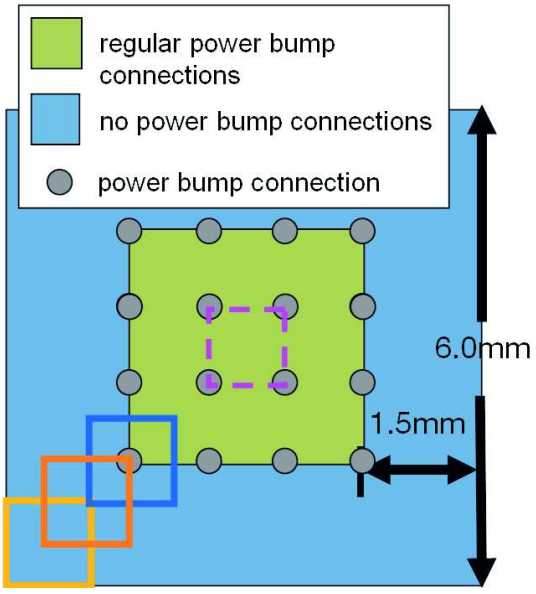

Fig. 4. Schematic of a SoC power grid, with regular power bump connections in the center and no package connections for power delivery in the outer (blue) region.

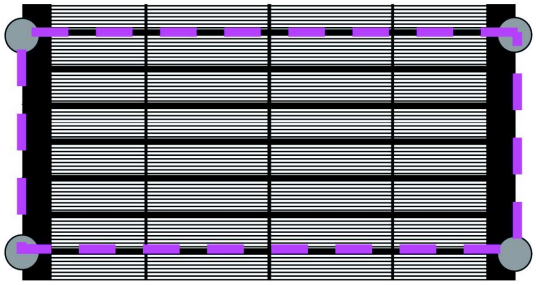

Fig. 5. Schematic of a on-chip grid with regular bump connections, top view of "regular grid".

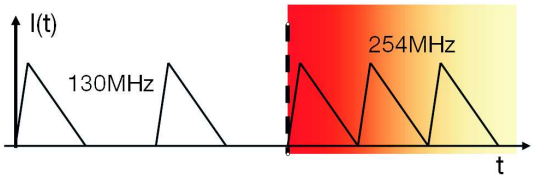

Fig. 6. Schematic of current profiles, emulating a frequency change from 130 MHz to 254 MHz, the colored area indicates the cycles of highest di/dt noise

before, a change of frequency from 130 MHz to 254 MHz was taken as di/dt noise event. The frequency change was emulated by applying current profiles as shown in Fig. 6 to the power grid. The colored area indicates the cycle in which the highest di/dt noise occurs. For simplicity an even current distribution over the entire core is assumed. In a post processing step the cycle and the position within the grid with the highest supply noise was determined.

4 Regular grid simulations

In the following section the simulation results for the "regular grid" will be discussed. To make a worst case estimation of the on-chip inductance, mutual inductances were omitted. This gives an upper bound for the inductance, since it assumes an infinitely wide current loop. In Fig. 7 the maximum transient drop of V_{supply} over the non switching cap, for a bump inductance L_{bump}=0.5nH, is displayed. The non switching capacitance is given by all gate and parasitic capacitances of, as well as the wiring connected to the non switching gates. The solid black lines are the simulation results for the two cases without on-chip inductance (L_0) and with the above mentioned worst case estimate of the on-chip inductance (L_{WC}). Their graphs are associated to the left y axis. On the right y axis the difference between the two black lines is plotted as dashed red line. Depending on the non switching capacitance, the difference is roughly between +100 mV and −10 mV, and therefore in the range of 10% of the absolute values. Therefore, on-chip inductance can have significant impact on the maximal voltage drop. This

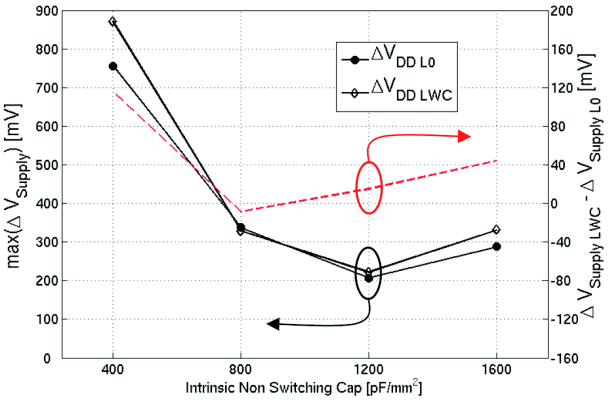

Fig. 7. Simulation results of maximum supply noise for varying intrinsic capacitance and resulting difference between simulations with worst case and zero on-chip inductance.

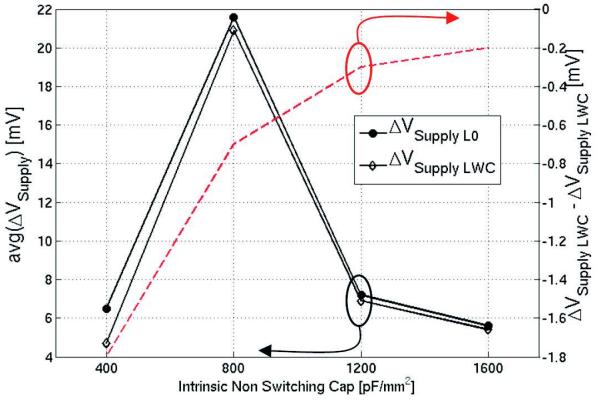

Fig. 8. Simulation results of cycle average of supply noise for varying intrinsic capacitance and resulting difference between simulations with worst case and zero on-chip inductance.

is in line with previous publications (Mezhiba and Friedman, 2004). Figure 8 displays, similar to Fig. 7, the maximum deviation of the cycle average of V_{supply}. Again, on the left y axis the simulation results for the two cases L_0 and L_{WC} are plotted. On the right axis the difference between the two cases is displayed. Comparing Fig. 8 and Fig. 7 yields two major differences. The first is that the absolute values are an order of magnitude smaller for the cycle average as they are for the maximum transient drop. Second, the difference between the two cases, indicated by the red dashed line, is much smaller for the cycle average not only in terms of absolute value but also for the relative deviation.

Therefore, even for a worst case estimation of on-chip inductance it has only a neglible effect on the cycle average of V_{supply} and therefore can be neglected in timing considerations. Figure 8 and Fig. 7 show the simulation results for L_{bump}=0.5 nH. For bump inductances of L_{bump}=0.75 nH and L_{bump}=1.0 nH similar results are obtained and are omit-

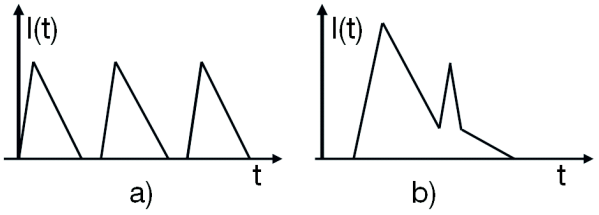

Fig. 9. More realistic current profiles **(a)** the current goes to zero by 90% of the cycle time **(b)** the current profile has a second peak caused by the falling clock edge.

ted here. As a next step, the impact of the current waveform was examined. Therefore, more realistic current profiles, as depicted in Fig. 9 were applied to the simulation setup. The modified current profiles resulted only into minimal changes of the simulation results.

5 SoC grid simulations

In this section a methodology for estimating the average effective inductance of the used ARM core is presented. Following this, simulation results of the SoC for the different inductance cases are presented and discussed.

5.1 Estimation of effective inductance

Initial simulations of the SoC grid showed a considerable deviation for the L_0 and the L_{WC} case even for the cycle average. Therefore, a more realistic estimate of the effective inductance was conducted. For this reason the wiring capacitance distribution of the ARM core, as depicted in Fig. 10, was used to estimate the wire length distribution of the core. The capacitance distribution in Fig. 10 is roughly a straight line on a double logarithmic scale. Hence, the distribution can be described as exponential function and therefore follows Rents Rule (Bakoglu, 1990), which makes it representative for most integrated circuit designs. This resulting wire length distribution was used to make conservative estimation for the effective inductance. To make the estimate as conservative as possible, these assumptions and simplifications were made: All wires with capacitances smaller than 4fF are omitted. With an estimated capacitance per micrometer of $C{=}150\frac{aF}{\mu m}$ this is equal to omitting all wires shorter than $26\mu m$. The chosen capacitance per micrometer is the smallest of all metal layers and leads to an overestimate of the wire length distribution, which in turn leads to an overestimate of the effective inductance. Additionally, for all nets a fanout of one, prohibiting branching and thus forcing maximum wire lengths, was assumed. Another simplification is that the load is assumed to be concentrated at the end of the wire, forcing maximal long current loops. Also a worst case orientation of all wires was assumed, again maximizing the possible current loop. The current distribution was again assumed to be

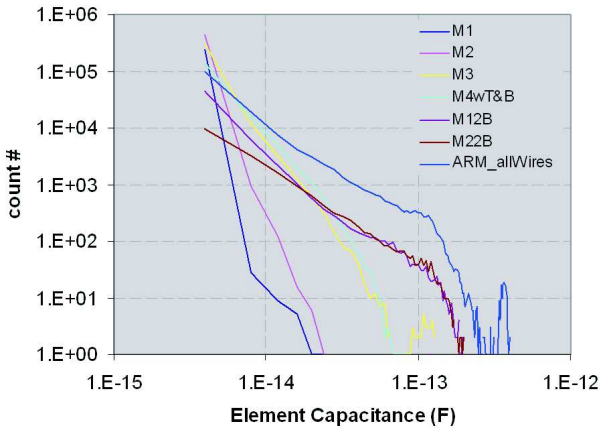

Fig. 10. Wiring capacitance distribution of the investigated ARM core. Capacitances smaller 4fF were omitted.

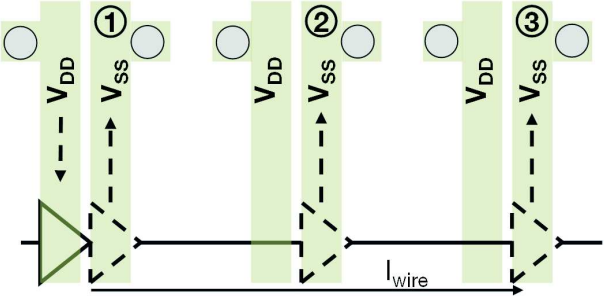

Fig. 11. Schematic for varying current return path with increasing wire length.

even, this might not be a worst case estimate, but was neccesarry for the feasibility of the study. With the resulting wire length distribution the probability for the different current return paths was calculated. In Fig. 11 a schematic is depicted, which shows a driving buffer, solid black triangular, and different load buffers, dashed black triangulars. Depending on the length of the connection, l_{wire}, from the driving to the load buffer the current return path can change from ① to ②, or ③. An inductance extraction for varying current return paths was conducted for all four metal layers used in the power grid wiring. The results are depicted in Fig. 12. The numbering for the current return paths was introduced since the pitches of the different metal layers vary over two orders of magnitude. The numbering was done according to Fig. 11. Figure 12 shows a steep increase of the inductance from the first to the second return path, followed by a saturation region where the inductance is almost independent on the current return path. This is due to the reason that only for the first current return path a strong inductive coupling between the V_{DD} and V_{SS} line exists, which decreases the effective inductance. Going to the second current return path increases the distance between the V_{DD} and V_{SS} line from

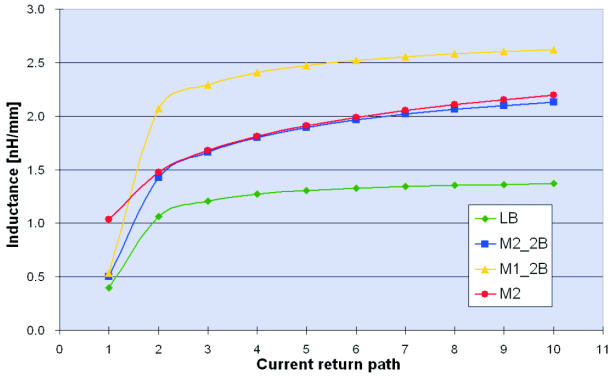

Fig. 12. Effective inductance for varying current return path. The x axis is the counted current return path starting at 1 for the direct return path, see Fig. 11.

Table 1. Probability of different current return paths and resulting effective inductance

		current return path				
		1	2	≥ 3	L_{eff}	L_{WC}
LB	pdf	99.2%	0.7%	0.1%		
	L [$\frac{nH}{mm}$]	0.4	1.2	1.4	0.41	1.91
M22B	pdf	82.6%	13.2%	4.2%		
	L [$\frac{nH}{mm}$]	0.5	1.4	2.1	0.68	2.1

a few hundreds of nanometers, spacing between neighboring lines, to tens or hundreds of micrometers, pitch of two pairs. The only metal layer where this effect does not exist is the lowest metal layer M2. This metal layer is used for the power wiring of the standard cells. Therefore, the minimal spacing of a V_{DD} and V_{SS} line is given by the standard cell height, which is in the range of a couple of micrometers. This leads to an increased minimum inductance. The results from Fig. 12 and the wire length distribution, derived from Fig. 10, are combined to a weighted mean which is then taken as effective inductance L_{eff}. In Table 1 the probability (pdf) of each current return path, the respective inductance of that return path, and the resulting effective inductance, as well as the worst case estimate (L_{WC}), which was used initially, are displayed for the metal layers LB and M22B. For the metal layer LB the effective inductance is L_{eff}=0.41$\frac{nH}{mm}$ which is almost identical to the inductance of the first current return path. For the M22B layer the effective inductance increases from the inductance of the first return path by 36% to L_{eff}=0.68$\frac{nH}{mm}$. Compared to the worst case estimate, L_{WC}, used earlier, the increase is still moderate. These inductance values are now used for the simulations in the SoC grid, the results are presented in the next section.

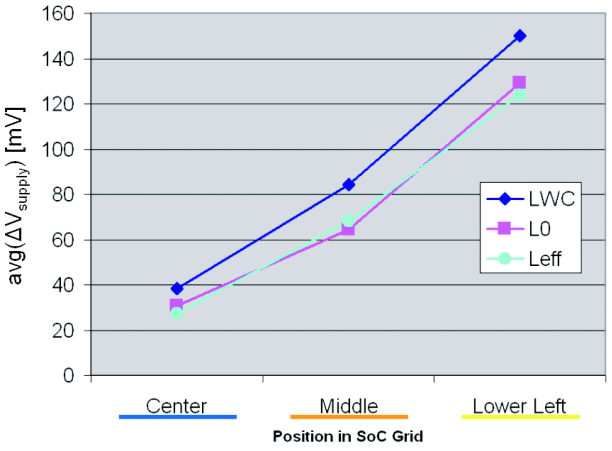

Fig. 13. Simulation results of the cycle average of supply voltage deviation, for varying core positions within the SoC grid and varying on-chip inductance values.

5.2 Simulation results

With the inductance values from Sect. 5.1 simulations in the SoC grid were performed. The simulation results are displayed in Fig. 13. On the x axis the possition within the SoC grid is plotted. The colored underlines relate to the colors used in Fig. 4. On the y axis the cycle average of the maximum supply voltage deviation is displayed for the three cases of no on-chip inductance (L_0), worst case estimate of on-chip inductance (L_{WC}), and effective inductance estimate of on-chip inductance (L_{eff}). It can be seen from Fig. 13 that for all three cases supply noise increase. This is due to the increased IR-Drop coming from the increased distance between core and the nearest power bump. The simulation results also show that an increase of up to 20 mV in cycle average power noise can be observed for L_{WC} compared to L_0. However, for the conservative estimate L_{eff} the cycle average of power noise is very close to L_0. The deviation is smaller than $\pm 5mV$ in absolute values and well below $\pm$5% normalized to the total noise budget. Since the on-chip inductance also in the SoC grid has a small impact on the cycle average of the power supply noise, it can also be neglected during timing considerations in SoC enviroments.

6 Conclusions

In this paper the effect of on-chip inductance on power supply integrity has been examined. Its effect on the maximum transient voltage drop as well as the impact on the cycle average of the supply voltage was presented. In accordance with previous publications, the impact of on-chip inductance on the maximum transient voltage drop was shown to be considerable. Therefore, on-chip inductance has to be taken into account during reliability considerations and on-chip signaling, for which the maximum value is of concern. However,

on-chip inductance was shown to have neglible effect on the cycle average of the supply voltage. This holds true for a grid with regular bump connections as well as for a grid scenario where there are no regular power bump connections. Therefore, on-chip inductance can be neglected during timing considerations of logic circuits for which the cycle average of the supply voltage and not the maximum voltage drop is the key metric.

References

Bakoglu, H. B.: Circuits, Interconnections, and Packaging for VLSI, Addison-Wesley Publication Company, 416–419, 1990.

Eireiner, M., Henzler, S., Missal, T., Berthold, J., and Schmitt-Landsiedel, D.: Power Supply Network Design: A Case Study Driven Approach, Adv. Radio Sci., URSI Kleinheubacher Berichte, 2006.

Kamon, M., Tsuk, M., and White, J.: FASTHENRY: a multipole-accelerated 3-D inductance extraction program, IEEE Transactions on Microwave Theory and Techniques, 1750–1758, 1994.

Larsson, P.: Power Supply Noise in Future IC's: A Crystal Ball Reading, IEEE Custom Integrated Circuits Conference, 467–474, 1999.

Lueftner, T., Berthold, J., Pacha, C., Georgakos, G., Sauzon, G., Hoemke, O., Beshenar, J., Mahrla, P., Just, K., Hober, P., Henzler, S., Schmitt-Landsiedel, D., Yakovleff, A., Klein, A., Knight, R., Acharya, P., Mabrouki, H., Juhoor, G., and Sauer, M.: A 90 nm CMOS Low-Power GSM/EDGE Multimedia-Enhanced Baseband Processor with 380 MHz ARM9 and Mixed-Signal Extensions, 2006 ISSCC Digest of Digital Papers, 252–253, 2006.

Mezhiba, A. and Friedman, E.: Inductive Properties of High-Performance Power Distribution Grids, IEEE Transactions on Very Large Scale Integraton (VLSI) Systems, 2002.

Mezhiba, A. V. and Friedman, E. G.: Scaling Trends of On-Chip Power Distribution Noise, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 12, 386–394, 2004.

N. Srivastava, X. Qi, K. B.: Impact of On-Chip Inductance on Power Distribution Network Design for Nanometer Scale Integrated Circuits, Proceedings of the Sixth International Symposium on Quality Electronic Design, 2005.

Nassif, S. R. and Fakhouri, O.: Technology Trends in Power-Grid-Induced Noise, in: Proceedings of the 2002 international workshop on System-level interconnect prediction, 55–59, ACM Press, 2002.

Saint-Laurent, M. and Swaminathan, M.: Impact of Power-Supply Noise on Timing in High-Frequency Microprocessors, IEEE Transactions on Advanced Packaging, 27, 135–144, 2004.