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A Fractional Ramp Generator with Improved Linearity and Phase-Noise Performance for the Use in Heterodyne Measurement Systems

T. Musch and B. Schiek

Institut für Hochfrequenztechnik, Ruhr-Universität Bochum, Universitätsstraße 150, 44780 Bochum, Germany

Abstract. Concepts for the generation and the measurement of highly linear frequency ramps are presented. The fractional ramp synthesiser concept shown here is able to generate frequency ramps with a very low phase noise level, a very good frequency linearity and reproducibility.

Related to the bandwidth of the generated frequency ramps of 4.5 GHz a relative linearity error below $4{\cdot}10^{-10}$ is demonstrated in a prototype system. This linearity error is close to the limit set by the phase noise floor of the ramp generators and marks a significant improvement over existing aproaches (Musch and Schiek, 2000). The basic measurement sensitivity due to the phase noise is $1.8{\cdot}10^{-10}$ without averaging.

As the phase noise is important for the linearity of the frequency ramp the set-up has to be optimised for a good phase noise behaviour, too. In order to achieve this good phase noise a special phase-frequency detector is introduced that is especially designed for the use in a fractional phase locked loop.

1 Introduction

The generation of extremely linear frequency ramps is important in high precision applications like heterodyne measurement systems. Industrial measurement systems often rely on fast, precise and additionally cost effective measurements. Highly linear frequency ramps offer the possibility of achieving those requirements altogether. One outstanding example of a measurement system with the highest demands for high precision frequency synthesis are accurate heterodyne vector network analysers (VNA).

Conventional vector network analysers are based on stepped frequency synthesisers which are quite easy to implement because static frequencies with a small frequency difference are simple to generate using standard phase-locked-loop (PLL) concepts. Since stepped frequency synthesisers are comparably slow when a high number of discrete frequencies is necessary, fast measurement systems benefit from analogue frequency ramps.

These dynamic frequency ramps are able to run quickly over a wide frequency band while at the same time they offer a high density of frequency samples. This is due to the fact that a ramp based system does not need the settling times of stepped frequency systems. In the VNA the analogue frequency ramps allow both for high speed measurements with a large number of frequencies being measured and a good accuracy on the condition that the frequency ramp generation is very stable.

Even more than absolute linearity errors of the frequency ramps, non-reproducible frequency ramps have detrimental effects on the measurement results in a VNA. Therefore a good reproducibility of the frequency ramps is the most important requirement of the ramp synthesisers besides a high ramp linearity. A reproducibility of the ramp frequency in the range of a few Hz is feasible. The fractional divider technique offers new solutions for highly linear, precise and robust ramp generators.

Key components (Schiek, 1999) of such fractional frequency ramp synthesisers are the division factor generation in the fractional frequency divider as well as the phase-frequency detector (PFD). The division factor generation is a completely digital part. Nevertheless the implemented algorithm generating the division factor sequence has a great influence on the overall phase noise performance of the whole system. A low division factor deviation (Musch and Schiek, 2001) is essential to reduce the noise-floor of the phase-frequency detector in the fractional mode of operation.

The PFD is a mixed digital/analogue component that directly and largely influences the phase noise behaviour of the synthesiser. This PFD has to operate extremely linearly, as it is very sensitive to the down-conversion of the unavoidable high-frequency fractional noise to non-filterable frequencies close to the carrier.

Finally, together with some compensation schemes, the ramp linearity is only limited by the phase noise level of the fractional PLL as stated below. This is the reason for the efforts made to reduce the phase noise level.

Correspondence to: T. Musch
(tom@hf.rub.de)

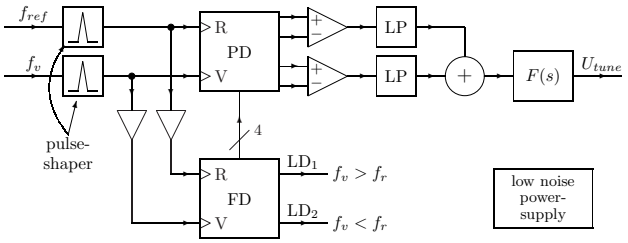

Fig. 1. Block diagram of the linear PFD with separated phase- and frequency detector.

2 A highly linear phase-frequency detector

Besides the broadband voltage controlled oscillator and the crystal reference oscillator, the key components in a fractional PLL are the fractional divider and the PFD.

The most important properties of the PFD are the linearity of the output voltage versus the input phase difference and the noise floor in the non-fractional mode of operation. The phase noise floor in the non-fractional mode marks the lower bound of the achievable phase noise in the fractional mode. The reason for this is the fact that the non-fractional phase noise is stochastically independent of the down-converted fractional noise, thus adding to the spectral power of the fractional noise.

The phase noise in the non-fractional mode of operation is mainly caused by analogue noise phenomena in the PFD-circuit while the fractional noise arises from the quasi-stochastic changes of the division factors of the fractional divider. In the strict sense the fractional noise is a deterministic phenomenon but since the periodicity is extremely long, in the range of several hours, it can be treated as a stochastic signal.

To achieve a low non-fractional phase noise behaviour it is important to use only low noise components in the critical signal path and to keep the critical signal path as simple as possible. In order to realise this, a separation of the phase detecting part responsible for the phase noise properties and the frequency detecting part only used during the pull-in process is applied in the PFD. The principle block diagram of the phase-frequency detector with the separation approach is shown in Fig. 1. The phase detector (PD) comprises two D-type flip-flops while the frequency detector (FD) is much more complex. The reference clock inputs R are fed by the pulse shaped signals from the reference oscillator e.g. a crystal controlled oscillator. The VCO-inputs V on the other are triggered by the output signals from the fractional divider which is located between the VCO and the PFD. The phase detector has a gain of

$$K_{pd} = \frac{4\,\mathrm{V}}{2\pi} \tag{1}$$

including the first mixed digital/analogue stage.

The frequency detector does not affect the gain of the phase detector. It consists of two blocks. One block is for the detection of large frequency differences to enable a fast lock process. The other block is a four-quadrant phase-follower. Both blocks are combined in the frequency detector (FD) block in Fig. 1 with the two lock detect outputs LD_1 and LD_2 indicating if the divided VCO-frequency f_v is higher or lower than the reference frequency f_{ref}. If the PLL is locked than both lock detect outputs are low.

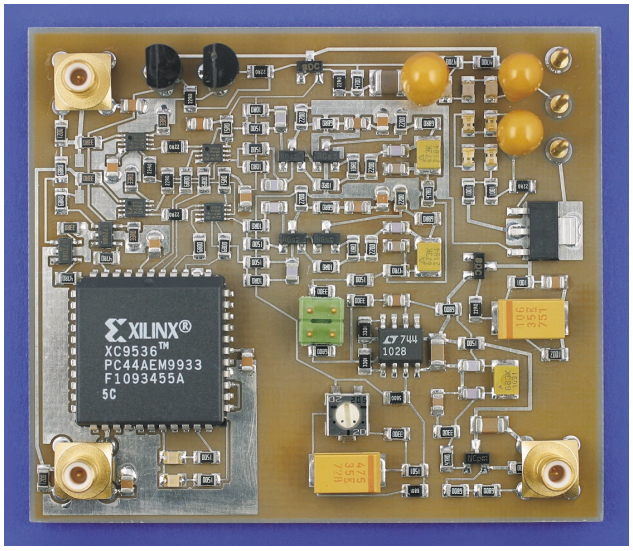

Fig. 2. Photography of the linear PFD with separated phase- and frequency detector.

In case that the phase is outside of the allowed range, the frequency detector intervenes upon the phase detector and forces the VCO in the desired direction. This is done by means of the control lines between the frequency detector and the phase detector. The control lines are not active when the PLL is locked so that no interferences and spurious signals are injected into the sensitive parts of the phase detector. As the frequency detector is quite complex and does not affect the phase noise, it is implemented in a complex programmable logic device (CPLD).

This separation enables the phase noise sensitive phase detector to be kept simple. Furthermore the phase detector part can be operated under optimal bias conditions regarding the phase difference thus exhibiting a very good linearity.

Besides this optimal phase bias a first highly linear mixed digital/analogue stage is necessary. To achieve the highest possible performance this part of the circuit is built with discrete components in a balanced structure. The balancing is used to suppress unwanted intermodulation products. Figure 2 shows a photography of the PFD circuit. The loop filter ($F(s)$) of the fractional PLL is also located on this circuit board to avoid crosstalk with other circuit parts. The loop filter contains the important low-pass filter that suppresses the higher noise frequencies of the fractional divider. Since the fractional divider produces strongly noisy signals at higher frequencies by nature, the low-pass filter is essential to block these fractional noise components from reaching the VCO.

The transfer function of the low-pass filter versus frequency has to be of a higher order than the shaped digital

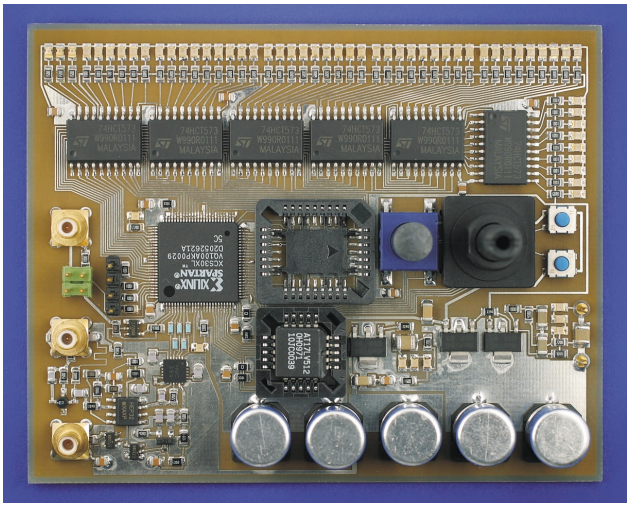

Fig. 3. Photography of the fractional divider circuit with the FPGA including the input and output components.

noise of the fractional logic thus suppressing the fractional noise even in the region of its steepest rise. As the fractional logic is of fourth order the overall low-pass characteristic of the loop filter is of fifth order.

A fundamental factor of the PLL is the theoretically lowest possible phase noise level that occurs in the non-fractional mode of operation. This phase noise floor $W^c_{\phi,pd}$ of the PFD related to the carrier is below

$$W^c_{\phi,pd} = -152\,\text{dBc/Hz}\,@\,5\,\text{kHz} \tag{2}$$

with a reference frequency at the PFD of 50 MHz. The PFD design is optimised for high comparison frequencies up to 100 MHz. But as the time jitter of the PFD above 50 MHz is nearly constant, an increase of the reference frequency above 50 MHz results in a decreasing phase noise level at the PFD. This decreasing phase noise level at the PFD has the effect that a higher reference frequency together with a lower division ratio in the frequency divider does not improve the phase noise level at the VCO significantly. The effect of the decreasing division factor is partly compensated by the rising phase noise level at the PFD.

3 A low noise fractional ramp division factor generator

Besides the PFD the fractional divider is of great importance for the noise performance of the fractional PLL and for the overall ramp linearity. Especially the division factor sequences are of great concern as they strongly influence the phase noise of the PLL.

In the prototype system the programmable microwave frequency divider together with the controller for the divider, which is implemented in a field programmable gate array (FPGA), as well as the complete input and display unit are located on one printed circuit board. Figure 3 depicts a photography of this fractional divider board. The FPGA is

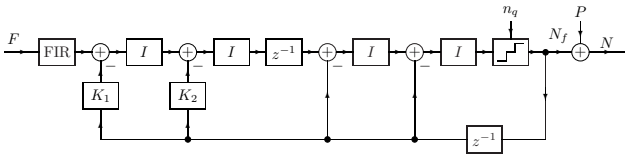

Fig. 4. Simplified block diagram of the four-stage fractional logic core with an additional delay element in the integrator chain.

surrounded by the input and display unit, the high frequency programmable divider, the flash memory, the serial EPROM and finally a low noise power supply. The FPGA generates the fractional division factors and contains the ramp generator as well as most parts of the input and display unit.

For the ramp generation several different methods are implemented. One is the internal linear ramp generation with a counter based ramp unit. This block is able to produce exactly linear frequency ramps without any additional frequency modulation on the ramp. If an additional frequency modulation is desired, another ramp mode based on a flash memory is used. This ramp mode allows for nearly arbitrary ramp shapes because the ramp curve is completely stored inside the memory.

As the flash memory is not able to handle clock frequencies in the range of 50 MHz or even more, an undersampling approach is chosen with a memory clock rate of a fourth of the fractional logic clock frequency. An additional interpolation stage calculates the missing interim values resulting in a smooth and highly accurate frequency curve. Besides the reduction of the memory clock rate the undersampling approach also reduces the memory space that is required to store one complete frequency ramp.

Since the division factors N of the programmable frequency divider are quite low in the range of

$$8 \leq N \leq 28 \tag{3}$$

the fractional logic should not have a high division factor deviation ΔN around the average fractional division factor $\bar{N}$. A large deviation ΔN would cause a high down-converted fractional noise. As a consequence, a simple sigma delta concept with cascaded integrator stages (, Racal, 1978,R) will not work properly. Therefore, a special fractional logic structure is used that generates fractional division factor sequences with a reduced deviation ΔN.

Additionally, the concept includes a pipelining structure that allows very high clock frequencies of the fractional logic core of more than 100 MHz. In practice, the maximum clock rate of the fractional logic is not the limiting factor for the reference frequency because the division factors would become too low with higher reference frequencies.

Average division factors below 12 are dangerous with respect to the down-conversion of the fractional noise. This is in fact the major limitation. Nevertheless, concerning the phase noise, it would not make much sense to move to higher reference frequencies because the time jitter of the PFD is nearly constant above 50 MHz.

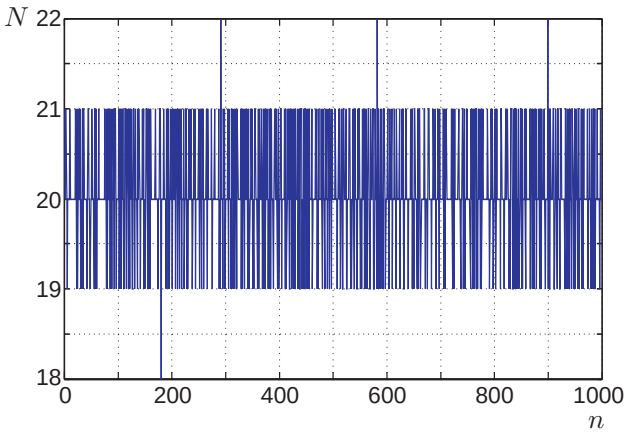

Fig. 5. Calculated part of a division factor sequence generated by the four-stage fractional logic.

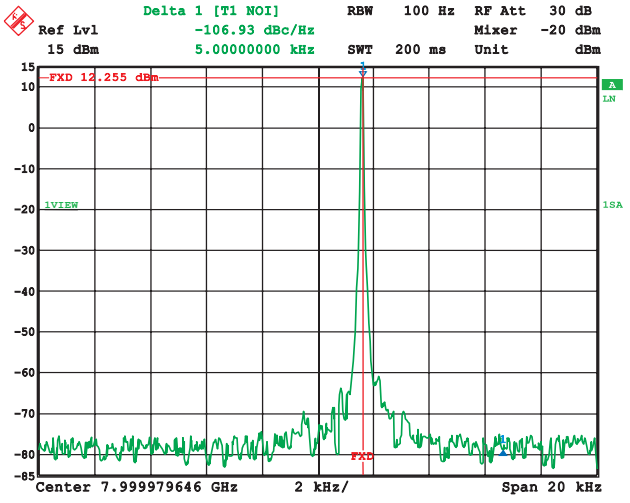

Fig. 6. Measurement of the phase noise level of the fractional PLL in the static mode.

The main idea behind the pipelining concept is to implement multiple delay stages in the fractional logic core. A simplified block diagram of a four-stage fractional core with two delay elements is shown in Fig. 4. The circuit behaviour is described using the z-Transform. The integrators I with the transfer function

$$I(z) = \frac{1}{1 - z^{-1}} \tag{4}$$

in the forward path are producing the noise shaping effect, which suppresses the fractional noise n_q close to the carrier.

The fractional noise n_q is caused by the quantisation at the output of the chain. The coefficients K_1 and K_2 have two essential tasks. Firstly, with the help of these coefficients the division factor deviation is reduced. Secondly, the coefficients are necessary to ensure a stable operation of the fractional logic.

A minimum of one delay element z^{-1} is necessary for a feasible digital feedback loop. By using one more delay element in the main signal path of the fractional core it is possible to synchronise the digital data stream inside the logic to the clock signal.

This is because of the additional delay element which breaks up the long chain of adders and integrators thus allowing for higher clock frequencies by roughly a factor of two. The FIR-filter in the input of the fractional logic compensates for the transfer function of the fractional logic except for a residual delay, which does not affect the performance of the fractional PLL.

Without the FIR-filter the transfer function of the fractional modulator chain in the z-domain can be derived from the block diagram in Fig. 4 as

$$N_f(z) = \frac{F(z)z^{-1} + n_q(z)D^4(z)}{V(z)} \tag{5}$$

where the denominator $V(z)$ is defined as

$$V(z) = D^3(z)K_2 + D^2(z)(1 - 2K_2 + K_1) + D(z)(K_2 - 2K_1) + K_1. \tag{6}$$

The time discrete transfer function of the differentiator $D(z)$ is given by

$$D(z) = 1 - z^{-1}. \tag{7}$$

A stability analysis is necessary to ensure a stable operation of the fractional logic. The two coefficients in the feedback path of the fractional logic are chosen to be

$$K_1 = 3/16, \tag{8}$$

$$K_2 = 1/2. \tag{9}$$

With these coefficients the system is working in the stable region. Besides the stability an important factor of the fractional logic is the amplitude of the division factor variation that is necessary to produce the mean fractional division ratios.

This division factor deviation strongly influences the down-conversion of the high-pass shaped fractional noise in the PFD. With the coefficients K_1 and K_2 the reduced peak to peak division factor deviation ΔN results in

$$\Delta N = 4. \tag{10}$$

This means that with an average division ratio $\bar{N}$=20.05 the division factors at the output of the fractional logic vary in a range between $18 \leq N \leq 22$. By way of a simulation an exemplary section of such a division factor sequence is shown in Fig. 5.

The division factors are shown versus the number n of clock cycles.

4 Measurements based on a dual fractional PLL ramp system

In order to verify the performance of the fractional PLL concept two categories of measurements are made with two prototype PLL circuits.

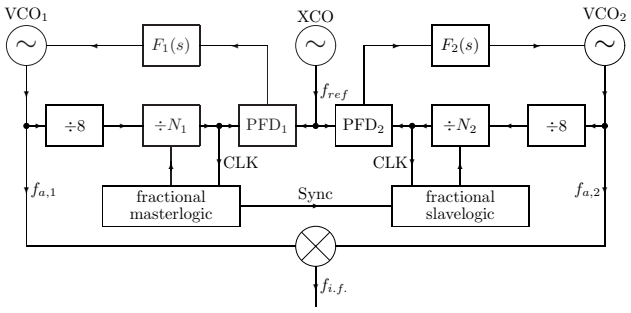

Fig. 7. Block diagram of the dual ramp system.

Firstly, to check the phase noise performance of the system a measurement with one of the two fractional PLLs is arranged in the static mode with a fixed frequency of roughly 8 GHz. A low phase noise spectrum analyser is used to directly record the spectrum close to the carrier from which the phase noise can be read. The result of this measurement is shown in Fig. 6. The phase noise level at an offset frequency of 5 kHz is in the order of -107 dBc/Hz. This is a very good result for a single loop fractional PLL with a VCO output frequency of 8 GHz.

The same measurement with the PLL in the non-fractional mode at an output frequency of exactly 8 GHz results in a phase noise level of -108 dBc/Hz at a 5 kHz offset frequency. This demonstrates the good linearity of the PFD because there is only 1 dB difference between the non-fractional mode, showing the minimum phase noise floor of the PLL, and the fractional mode that adds additional fractional noise, which is down-converted due to the non-linearity of the PFD characteristic.

The good phase noise behaviour is relying on both a highly linear PFD and additionally a fractional logic offering a low division factor deviation. Together with a high reference frequency a good ramp linearity is feasible, which is finally limited by the phase noise of the PLLs.

From the phase noise level at the output of the VCO it is possible to calculate the equivalent phase noise level at the PFD operating at 50 MHz. The phase noise level at the PFD referred to the carrier results in

$$\begin{aligned} W^c_{\phi,pd}(5\,\mathrm{kHz}) &= \frac{W^c_{\phi,vco}(5\,\mathrm{kHz})}{\bar{N}^2} \\ &= -108\,\mathrm{dBc/Hz} - 10\log(\bar{N}^2) \\ &= -152\,\mathrm{dBc/Hz}. \end{aligned} \tag{11}$$

This phase noise level comprises the phase noise influences of the divider and the crystal oscillator, too. Therefore, the noise floor of the PFD is well below -152 dBc/Hz.

To measure the ramp linearity a dual loop set-up is used. The dual loop approach allows for highly sensitive measurements with a frequency resolution of some hundred mHz. The idea is to run two extremely linear frequency ramps in parallel and down-convert the difference frequency to an i.f.-signal. The frequencies of the i.f.-signal are in the range of some kHz and can easily be sampled in an analogue to digital converter (ADC).

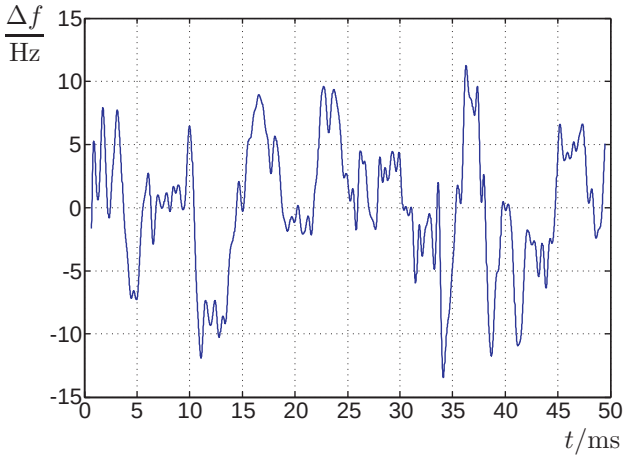

Fig. 8. Measured frequency deviation between the two parallel frequency ramps.

The block diagram of the dual loop system is depicted in Fig. 7.

At the output of the mixer the i.f.-signal is present at a low intermediate frequency of

$$f_{i.f.} = |f_{a,2} - f_{a,1}| \approx 3\,\mathrm{kHz}. \tag{12}$$

After a low pass filtering of the i.f.-signal to keep the microwave frequencies of the ramps away from the next signal processing stages, the i.f.-signal is sampled in an analogue to digital converter. Then, the data can be processed in a computer.

For a highly sensitive signal processing the spectrum of the i.f.-signal is calculated first by means of a Fourier transform. Within the i.f.-spectrum a certain bandwidth around the i.f. spectral peak is filtered. This bandwidth has to be chosen properly in order to include all relevant spectral sidebands carrying information about the non-linearity. If, on the other hand, the bandwidth is wider than necessary the noise on the i.f.-signal reduces the sensitivity of the measurement. The filter bandwidth in the following measurements is chosen as 2 kHz.

The spectrum at negative frequencies is set to zero and the complex analytical time signal is calculated via an inverse Fourier Transform. The derivative of the angle of this complex analytical time signal is equal to the frequency deviation between the two frequency ramps. To ensure the relevance of the linearity measurement an unwanted synchronicity between the two ramps has to be avoided.

To ensure this the measurement set-up comprises for example different VCOs and different fractional divider sequences thus suppressing ganging effects. Figure 8 shows the result of such a linearity measurement with the two VCOs running from 4.5 GHz up to 9 GHz with a ramp bandwidth of

$$B_r = 4.5\,\mathrm{GHz} \tag{13}$$

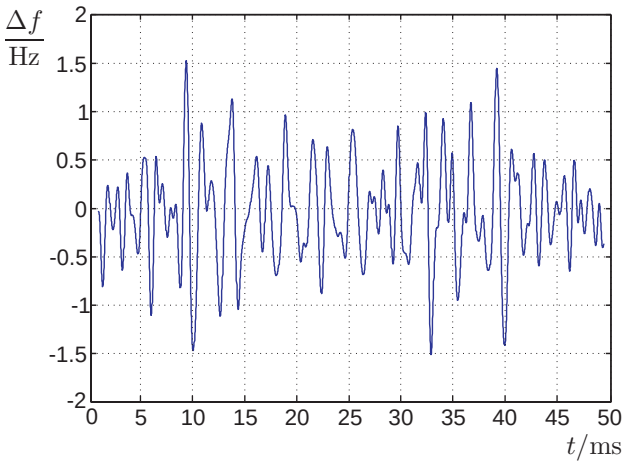

Fig. 9. Measured frequency deviation between the two frequency ramps using the frequency error compensation.

and a ramp time of

$$T_r = 50\,\text{ms} \tag{14}$$

having a difference frequency $f_{\text{i.f.}}$ of roughly 3 kHz. The maximum frequency error is in the order of ±13 Hz. Related to the bandwidth this results in a relative non-linearity of $2.9{\cdot}10^{-9}$.

With the realistic assumption that both fractional ramp PLLs show uncorrelated frequency deviations from the ideal ramp with approximately the same magnitude, the non-linearity of each ramp generator results as $1/\sqrt{2}$ times the deviation measured in Fig. 8. The estimated non-linearity of each ramp is in the order of $2.1{\cdot}10^{-9}$. This is already a very good ramp linearity.

In order to illustrate the potential of the fractional ramp concept the measured frequency error in Fig. 8 can be used to frequency modulate one of the fractional ramp PLLs with the inverse frequency error to compensate for it. After this compensation a new linearity measurement is carried out and the result is shown in Fig. 9. The frequency error after implementing the compensation is in the range of ±1.5 Hz. Thus the relative non-linearity is better than $3.4{\cdot}10^{-10}$.

A further interesting question concerns the sensitivity of the measurement and the influence of the phase noise. Therefore the same non-linearity evaluation can be performed when both PLLs are working in the static mode having fixed frequencies and a fixed difference frequency because no linearity error can influence the measurement result in this case. The only factor to be taken into consideration is the phase noise.

With the result from the phase noise measurement in Fig. 6 it is possible to estimate the frequency error with the measurement method described above.

The first step is to calculate the phase noise of the i.f.-signal. The mixing of two signals with uncorrelated noise contributions increases the phase noise level by 3 dB compared to the phase noise of each individual oscillator. Furthermore, the i.f.-frequency is much smaller than the loop bandwidth of the PLL of roughly 400 kHz.

The two frequencies at the mixer are so close to each other that the uncorrelated phase noise from both sidebands is down-converted to the i.f.-signal thus further reducing the phase noise level by 3 dB. From this the expected phase noise level of the i.f.-signal is

$$\begin{aligned} W^c_{\phi,i.f.}(5\,\text{kHz}) &= -107\,\text{dBc/Hz} + 6\,\text{dB} \\ &= -101\,\text{dBc/Hz}. \end{aligned} \tag{15}$$

With some additional noise from the ADC and the i.f.-amplifier the overall i.f.-phase noise level could be slightly higher.

For the further calculations the knowledge of the shape of the i.f.-phase noise spectrum is necessary. As a PLL shows a white spectrum well below the cut-off frequency of the closed loop it is quite easy to describe the shape of the i.f.-spectrum. Including the flicker noise corner frequency ω_c the i.f.-phase noise spectrum can be described as

$$W^c_{\phi,i.f.}(\omega_{of}) = \left|1 + \frac{\omega_c}{\omega_{of}}\right| \cdot W^c_{\phi,i.f.}(5\,\text{kHz}). \tag{16}$$

The value of interest that can be compared with the results of the linearity measurements in Figs. 8 and 9 is the variance of the i.f.-frequency as calculated from the analytical time signal within the filter bandwidth of 2 kHz.

To derive this value the energy of the frequency noise within the filter bandwidth of 2 kHz has to be evaluated. Therefore, at first the frequency spectrum is calculated from the phase noise spectrum in Eq. (16) to be

$$W^c_{\omega,i.f.}(\omega_{of}) = \left|1 + \frac{\omega_c}{\omega_{of}}\right| \cdot \omega^2_{of} \cdot W^c_{\phi,i.f.}(5\,\text{kHz}). \tag{17}$$

From this frequency noise spectrum the variance $\sigma^2_{\omega,\text{i.f.}}$ of the i.f.-frequency results from an integration over the filter bandwidth as

$$\begin{aligned} \sigma^2_{\omega,i.f.} &= \frac{1}{2\pi} \int_{-\omega_g}^{\omega_g} \left|1 + \frac{\omega_c}{\omega_{of}}\right| \\ &\quad \cdot W^c_{\phi,i.f.}(5\,\text{kHz}) \cdot \omega^2_{of} \cdot d\omega_{of} \\ &= \frac{1}{\pi} W^c_{\phi,i.f.}(5\,\text{kHz}) \left(\frac{\omega^3_g}{3} + \omega_c \frac{\omega^2_g}{2}\right). \end{aligned} \tag{18}$$

With the variance $\sigma^2_{\omega,i.f.}$ the standard deviation $\sigma_{f,\text{i.f.}}$ of the i.f.-frequency in Hz can be calculated directly resulting in

$$\begin{aligned} \sigma_{f,i.f.} &= \frac{1}{2\pi} \sigma_{\omega,i.f.} \\ &= \frac{1}{2\pi} \sqrt{\frac{1}{\pi} W^c_{\phi,i.f.}(5\,\text{kHz}) \left(\frac{\omega^3_g}{3} + \omega_c \frac{\omega^2_g}{2}\right)}. \end{aligned} \tag{19}$$

With the value of −101 dBc/Hz for the i.f.-phase noise level at 5 kHz offset frequency, a cut-off frequency

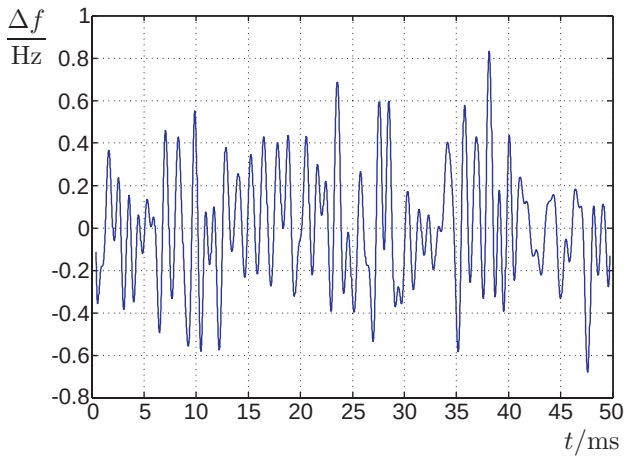

Fig. 10. Measured frequency deviation between the two frequency generators in the fixed frequency mode.

$\omega_g = 2\pi\,1000\,\text{Hz}$ of the filter in the i.f.-spectrum and a flicker-noise corner frequency $\omega_c = 2\pi\,300\,\text{Hz}$ the standard deviation of the i.f.-frequency results as

$$\sigma_{f,i.f.} \approx 0.28\,\text{Hz}. \tag{20}$$

This theoretically predicted value can be compared to a measurement with the dual ramp system in the static frequency mode, with only the phase noise influencing the result.

Figure 10 shows the measured frequency deviation of the i.f.-signal versus time in the static mode with the fixed frequency set to 8 GHz like in the phase noise measurement of Fig. 6. The time axis as well as the filter parameters for the digital filter in the i.f.-spectrum are the same as for the ramp measurements in order to ensure the significance of the measurement. The maximum frequency deviation is below ± 0.8 Hz with a measured standard deviation of 0.27 Hz. This standard deviation is quite close to the theoretically calculated value of Eq. (20).

The frequency deviation in Fig. 10 is the lower bound of the ramp linearity that is achievable with a dual ramp generator including two ramp generators with a phase noise level of roughly -107 dBc/Hz. This lower bound corresponds to a relative ramp non-linearity between the two ramps of $1.8 \cdot 10^{-10}$ referred to a ramp-bandwidth of 4.5 GHz.

5 Conclusion

A concept for the generation of extremely linear frequency ramps is presented that improves the linearity by more than a factor of ten compared to existing systems. This is achieved by using firstly a low phase noise fractional PLL. The low noise values are obtained by a special low noise PFD with an extremely high linearity of the phase-to-voltage conversion.

Secondly, a FPGA based fractional core allowing for high reference frequencies with a small division factor deviation is a key component. This fractional FPGA allows for a large number of division factors on the ramp due to the high reference frequency. A large number of divider steps on the ramp is the key factor for a low non-linearity while the small division factor deviation reduces the down-conversion of the fractional noise thus reducing the phase noise of the fractional PLL.

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