



High-voltage circuits for power management on 65 nm CMOS

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Abstract. This paper presents two high-voltage circuits used in power management, a switching driver for buck converter with optimized on-resistance and a low dropout (LDO) voltage regulator with 2-stacked pMOS pass devices. The circuit design is based on stacked MOSFETs, thus the circuits are technology independent.

High-voltage drivers with stacked devices suffer from slow switching characteristics. In this paper, a new concept to adjust gate voltages of stacked transistors is introduced for reduction of on-resistance. According to the theory, a circuit is proposed that drives 2 stacked transistors of a driver. Simulation results show a reduction of the on-resistance between 27 and 86 % and a reduction of rise and fall times between 16 and 83 % with a load capacitance of 150 pF at various supply voltages, compared to previous work. The concept can be applied to each high-voltage driver that is based on a number (N) of stacked transistors.

The high voltage compatibility of the low drop-out voltage regulator (LDO) is established by a 2-stacked pMOS transistors as pass device controlled by two regulators: an error amplifier and a 2nd amplifier adjusting the division of the voltages between the two pass transistors. A high GBW and good DC accuracy in line and load regulation is achieved by using 3-stage error amplifiers. To improve stability, two feedback loops are utilized.

In this paper, the 2.5 V I/O transistors of the TSMC 65 nm CMOS technology are used for the circuit design.

of standard device interfaces and batteries. Thus one common method to design high-voltage circuits is to use high-voltage transistors, which are technology dependent (Bandyopadhyay et al., 2011). In contrast, high-voltage circuits based on stacked low-voltage CMOS transistors are more efficient because of their full compatibility with scaled technologies (Serneels and Steyaert, 2008; Nam et al., 2012; Bradburn and Hess, 2010).

High voltage circuits using stacked devices are a problem, when fast switching or high currents are required. Therefore this paper summarizes the design of two important high voltage circuits for power management, a driver for switching applications (Pashmineh et al., 2013b, c) and a low-dropout voltage regulator (Pashmineh et al., 2013a), both based on stacked transistors. The voltage between terminals of each transistor have been kept within the technology limit.

This work is organized as follows: Sect. 2 describes the structure and operation of a high-voltage driver based on stacked standard CMOS transistors. For reducing the on-resistance of drivers, a theory to calculate gate voltages of stacked transistors to drive the maximum drain current is presented. According to the theory a circuit design methodology is described to generate these voltages. Section 3 introduces the structure and operation of an LDO based on 2-stacked pMOS pass transistors. The circuit design of two regulators, which control the pass transistors, thus regulate the output and the voltages between the two pass devices, is described. Section 4 presents the simulation results of the proposed LDO and a 2-stacked CMOS driver in 65 nm TSMC technology. The results demonstrate a significantly low dropout voltage of the LDO and considerably improved rise and fall times of the driver. Finally, conclusions are given.

1 Introduction

Power management plays an increasing role in electronic systems for consumers, sensors and automotive electronics. However, the standard transistors of nanometer CMOS technologies are only capable to handle low voltages within technology limits and are therefore not compatible with voltages

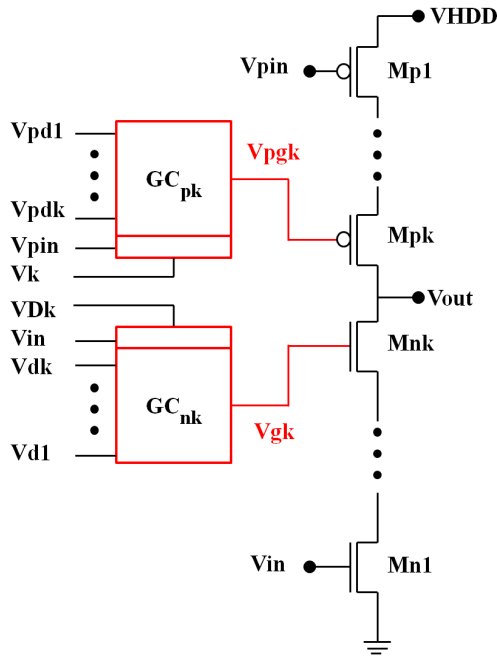


Figure 1. A high-voltage N -stacked CMOS driver circuit.

2 Drivers

Drivers are one of the most important circuit blocks used in power management to switch converters and amplifiers.

In this paper, the proposed high-voltage drivers are based on stacked low-voltage standard CMOS transistors and are technology independent. Their disadvantage however, is that depending on the number of stacked transistors, switching speed may not satisfy requirements because of raised on-resistance of the pull-up and pull-down driver transistors, resulting in slower charge and discharge characteristics of capacitive output nodes.

This work focuses on reduction of the on-resistance of high-voltage drivers. In the following sections a new circuit topology for high-voltage drivers with a minimum on-resistance will be introduced.

2.1 System description

A high-voltage driver based on stacked low-voltage standard CMOS transistors is shown in Fig. 1.

The number of stacked transistors depends on the supply voltage, because the voltage between the terminals of each standard transistor has to be equal to or less than the nominal operating voltage V_n . With a supply voltage of V_{HDD} , which is in the range of $(N - 1) \times V_n$ to $N \times V_n$, the high-voltage driver was designed using N stacked CMOS transistors (N pMOS transistors in the pull-up and N nMOS transistors in the pull-down path).

The driver is controlled by two input signals. The first is V_{in} , which varies between the ground and the nominal oper-

ating voltage V_n and switches the first nMOS transistor M_{n1} . The second input signal V_{pin} , which is level shifted from V_{in} and varies between $V_{HDD} - V_n$ and V_{HDD} , switches the first pMOS transistor M_{p1} .

The main challenge in designing high-voltage drivers is the generation of gate voltages of cascode transistors of the stack ($M_{n2} \dots M_{nk}$, $M_{p2} \dots M_{pk}$), which need to fulfil two requirements.

First, the transistor in the stack of the driver output must be switched in a way that the voltage between the terminals of each transistor is kept within the technological limits. Second, the driver should pull-up and pull-down with the maximum possible current by setting the appropriate gate voltages for each of the N -stacked transistors. Such a driver realizes a minimum on-resistance.

Therefore a theory describing the optimal gate drive voltages of the N -stacked transistors must be developed.

According to the theory, external circuits (GC_{nk} and GC_{pk}) have been designed to generate these voltages (Fig. 1). This will be fully described in the following sections.

2.2 Circuit theory

In this paper, the gate voltages of N -stacked transistors of a high-voltage driver, except for the first CMOS transistors which are switched by the input signals, have been calculated using a computer algebra system for each output voltage.

First, the gates of the N -stacked nMOS transistors of the pull-down path are considered.

The calculation has been performed for both closed (1) and open (2) scenarios:

1. Operation in on-condition for a maximum drain current at an input signal of 2.5 V, which switches the driver on. The gate voltages of nMOS transistors have been calculated to switch the corresponding nMOS transistors on, enabling a maximum drain current and a minimized on-resistance of the pull-down path. As a result the driver's output can be discharged to the ground.
2. Operation in off-condition at an input signal of 0 V, which switches the first nMOS transistor off. The calculated gate voltages of this condition turn off the respective nMOS transistors. As a consequence, the output can be charged to the high-voltage V_{HDD} .

In both cases, the voltages between each transistor's terminals were kept within the technologically required range.

In the next sections, both conditions are described in further detail.

2.2.1 Operation in on-condition

In this case, the input signal is logical high, which is 2.5 V in this work, turning transistor M_{n1} on. The gate voltages of the other transistors have been calculated to switch the

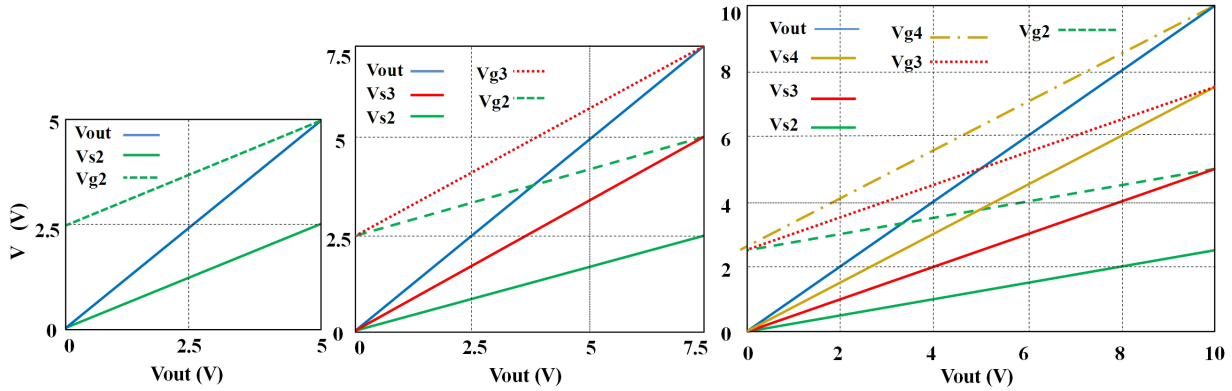


Figure 2. Node voltages characteristics of a (a) 2- (b) 3- (c) 4-NMOS driver for a maximum drain current (on-condition).

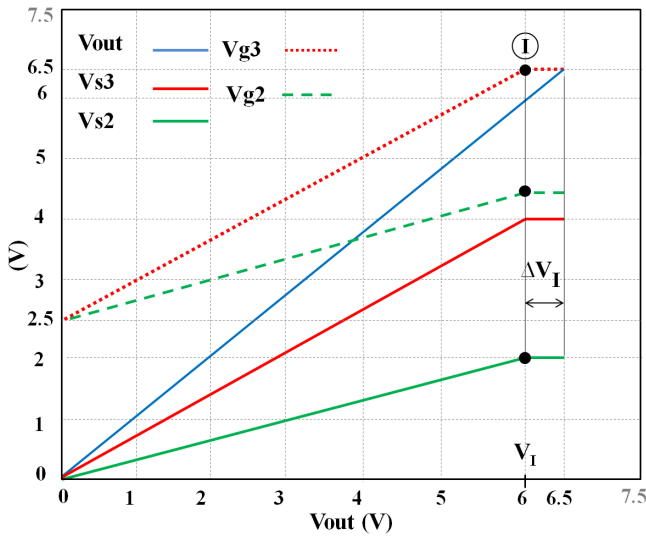


Figure 3. Node Voltages of 3-stacked NMOS driver (on-condition, VHDD = 6.5 V.)

corresponding transistors on and also to drive a maximum drain current. The driver output is discharged from the high-supply voltage VHDD to the ground.

The characteristics of the calculated gate voltages of 2-, 3- and 4-stacked nMOS devices are mapped over the driver output voltages for maximum drain currents as depicted in Fig. 2a, b and c. The driver has a high supply voltage, which is N times greater than the nominal operating voltage V_n . Depending on the number of driver stacked nMOS, the output node V_{out} is discharged from 5, 7.5 and 10 to 0 V.

The calculated results prove that the source node voltage of each nMOS transistor is proportional to the driver's output voltage. The gate terminal has an offset to the source voltage, which is equal to the nominal operating voltage (2.5 V). Due to this, the gate, drain and source voltage of each nMOS transistor can be described as functions of the output voltage, as

shown in the following equations:

$$V_{sk} = \frac{(k-1) \times V_{out}}{N}, \quad k \geq 2 \quad (1)$$

$$V_{gk} = \frac{(k-1) \times V_{out}}{N} + 2.5 \text{ V}, \quad k \geq 2 \quad (2)$$

$$V_{dk} = \frac{k \times V_{out}}{N}, \quad k \geq 2 \quad (3)$$

N stands for the total number of nMOS transistors; V_{sk} , V_{gk} and V_{dk} denotes source, gate and drain node voltages of the k th nMOS transistor respectively, as shown in Fig. 1.

According to the above equations, the relations between node and output voltages of a 3-stacked nMOS driver can be expressed with the following conditions:

$$V_{s2} = \frac{V_{out}}{3}, \quad V_{s3} = \frac{2 \times V_{out}}{3} \quad (4)$$

$$V_{g2} = \frac{V_{out}}{3} + 2.5 \text{ V}, \quad V_{g3} = \frac{2 \times V_{out}}{3} + 2.5 \text{ V} \quad (5)$$

$$V_{d2} = \frac{2 \times V_{out}}{3}, \quad V_{d3} = \frac{3 \times V_{out}}{3} = V_{out} \quad (6)$$

V_{s2} and V_{s3} are the source, V_{g2} and V_{g3} the gate and V_{d2} and V_{d3} the drain node voltages of the 2nd and 3rd nMOS transistor respectively. The above relations of node voltages correspond with the calculation results of a 3-stacked nMOS driver in Fig. 2b.

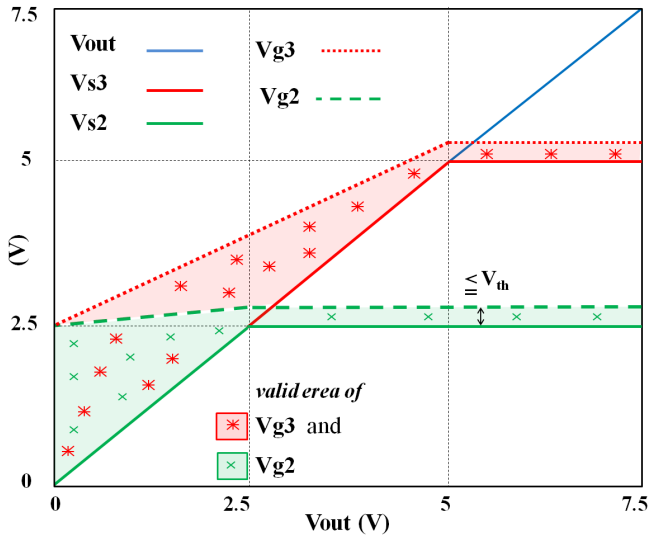
The gate voltages are calculated for a driver with a high supply voltage, which is N -times greater than the nominal operating voltage V_n .

From the calculation results of the required gate voltages of an N -stacked nMOS driver with a supply voltage different from $N \times V_n$, the following expression can be obtained:

$$\begin{cases} V_{gN} = V_{HDD} \\ V_{gk} = k \times V_n - \Delta V_I, & V_{out} > V_I, \quad 2 \leq k < N \\ V_{gk} = \frac{(k-1) \times V_{out}}{N} + 2.5 \text{ V}. & V_{out} \leq V_I \end{cases}$$

Table 1. ΔVI of a 2, 3 and 4-stacked driver with various supply voltages.

2-stacked driver		3-stacked driver		4-stacked driver	
VHDD [V]	ΔVI [V]	VHDD [V]	ΔVI [V]	VHDD [V]	ΔVI [V]
5.0	0.0	7.5	0.0	10.0	0.0
4.5	0.5	7.0	0.25	9.5	0.125
4.0	1.0	6.5	0.5	9.0	0.25
3.5	1.5	6.0	0.75	8.5	0.375
3.0	2.0	5.5	1.0	8.0	0.5

**Figure 4.** Node Voltages of 3-stacked NMOS driver (off-condition).

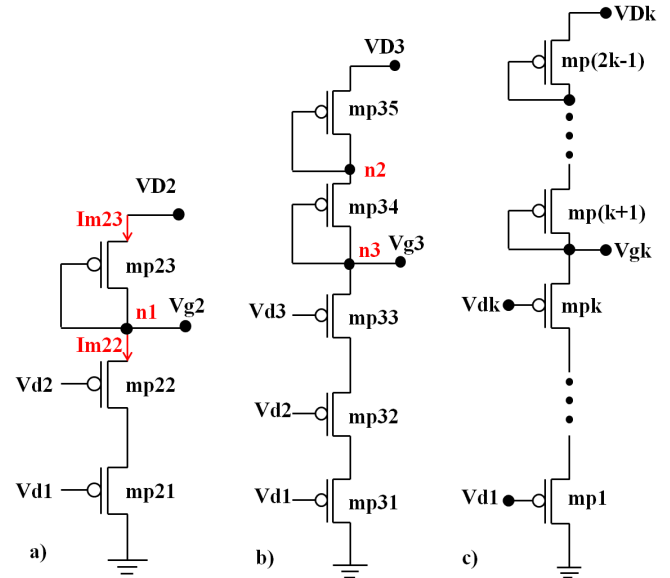
(7)

VI is the voltage of the point I, as can be seen in Fig. 3. At the beginning of the discharge of the output and pull-down nodes, the gate voltage of each nMOS transistor is constant down to point (I). When the discharge of the driver output falls below this point, the source and gate voltages follow the rule according Eqs. (1) and (2).

Table 1 shows the results of ΔVI , the difference between the supply voltage and VI. By increasing the number of stacked nMOS-transistors, ΔVI decreases. This means that the gate voltages follow the rule (1) for higher N -stacked nMOS.

With an input signal of 0 V, which switches the first nMOS transistor off, the input signal of the pull-up path V_{pin} is equal to $V_{HDD} - V_n$, which switches the first pMOS transistor on.

The gate voltages of the other pMOS transistors have been calculated for switching the corresponding transistor on and also driving a maximum drain current in the pull-up path to charge the output from the ground to the high-supply voltage V_{HDD} .

**Figure 5.** (a) Circuits to generate gate voltages V_{g2} , (b) V_{g3} and (c) V_{gk} .

The calculated results of gate and source voltages of the pMOS transistors, which are related to the output voltage, can be described with the following functions:

$$V_{psk} = \frac{(k_p - 1) \times V_{out}}{N} + (N + 1 - k_p) \times 2.5 \text{ V},$$

$$k_p \geq 2 \quad (8)$$

$$V_{pgk} = V_{psk} - 2.5 \text{ V} \Rightarrow V_{gk} = \frac{(k_p - 1) \times V_{out}}{N}$$

$$+ (N - k_p) \times 2.5 \text{ V}, \quad k_p \geq 2. \quad (9)$$

Number k_p denotes the k th pMOS-transistor of the high-voltage driver.

2.2.2 Operation in off-condition

In off-condition the input signal V_{in} is 0 V, which switches the first nMOS transistor off. The gate voltages of the other nMOS transistors need to be adjusted in such a way that the corresponding transistors can be switched off as quickly as possible in order to avoid shot-through currents in the push-

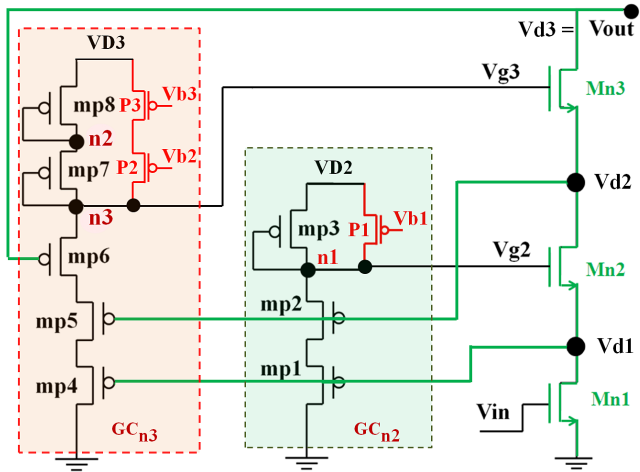


Figure 6. Circuits to generate gate voltages of a 3-stacked NMOS driver.

pull driver and to maintain the voltage between the nodes of each transistor within the technology limit. As a result, the output load will be charged with the highest possible rate.

To meet the above conditions, a stacked transistor must be switched off, if the source node voltage rises to the limit:

$$V_{sk_limit} = (k - 1) \times \frac{V_{HDD}}{N}. \quad (10)$$

In the off-state of each transistor, the gate-source voltage must be equal to or less than the threshold voltage.

Figure 4 shows the calculated gate and source voltages of a 3-stacked nMOS driver with a supply voltage of 7.5 V. The second nMOS transistor switches off at an output voltage of 2.5 V and the third at 5 V. Finally the driver output node is charged to 7.5 V.

2.3 Circuit design

A circuit design methodology for generation of voltages according to the theoretical results is described in this section.

The circuit that generates the gate voltages of the 2nd nMOS transistor V_{g2} is depicted in Fig. 5a. As can be seen, the circuit is supplied by $VD2$ and contains 3 pMOS transistors ($mp21$, $mp22$ and $mp23$) in series. The transistor $mp23$ is gate-drain connected and the gate nodes of the other transistors are determined by the voltages of the driver nodes V_{d1} and V_{d2} (drain voltages of the driver transistors $Mn1$ and $Mn2$ in the pull-down path). The dimensions of $mp21$ have been set for operation of transistor $mp22$ in saturation region during the on-condition. The dimensions of the transistors $mp22$ and $mp23$ are the same. Therefore, node $n1$ between $mp22$ and $mp23$ (Fig. 5a) supplies the required gate voltage V_{g2} . According to the on- and off-conditions, the supply voltage of this circuit ($VD2$) switches between $5V - \Delta VI$ and $2.5V$ respectively. The value of ΔVI depends on

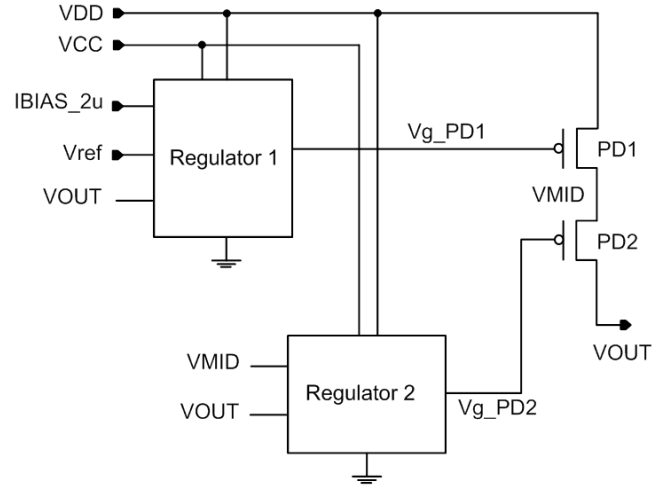


Figure 7. Principle of a LDO with two cascaded pass devices PD1 and PD2.

the high-supply voltage of the driver and can be read from Table 1.

The expression in Eq. (10) describes the required voltage of V_{g2} during the on-condition. It is derived from two equations with equal drain currents of $mp22$ and $mp23$ in the saturation region.

$$\left. \begin{aligned} I_{mp23} &= \frac{\beta_p}{2} \times (VD2 - V_{g2} - V_{thp})^2 \\ I_{mp22} &= \frac{\beta_p}{2} \times (V_{g2} - V_{d2} - V_{thp})^2 \end{aligned} \right\} \begin{aligned} (3): \quad V_{d2} &= \frac{2 \times V_{out}}{N} \\ \Rightarrow & \end{aligned}$$

$$V_{g2} = \frac{V_{out}}{N} + \frac{VD2}{2}. \quad (11)$$

In the on-condition, when the high supply voltage of driver V_{HDD} is N times greater than the nominal voltage V_n , the supply voltage ($VD2$) of the gate-control circuit GC_n2 switches to 5 V. The generated voltage V_{g2} from Eq. (10) is equal to the calculated gate voltage of the second stacked nMOS transistor, as in Eq. (2).

The current I_{mp23} of the transistor $mp23$ begins to flow when the gate-source voltage of $mp23$ exceeds its threshold voltage. In this case, the desired voltage of 5 V at node $n1$ is limited to $5V - V_{th}$. To solve this problem, a pMOS transistor (such as $P1$ in Fig. 6) has been connected in parallel to $mp3$. The gate of this transistor ($P1$) is biased by V_{b1} . When the nominal voltage is not an exact fraction of the high supply voltage V_{HDD} , this parallel pMOS transistor ($P1$) enables the generated voltage at the node $n1$ to approach the conditions in Eq. (7).

Figure 5b shows a circuit generating the gate voltage (V_{g3}) of the third nMOS transistor. This gate control circuit GC_n3 comprises 5 pMOS transistors ($mp31$ - $mp35$) in series, with a supply voltage $VD3$, which switches between $7.5V - \Delta VI$ and $5V$, respectively, according to the on- or off-conditions. Both transistors $mp34$ and $mp35$ are gate-

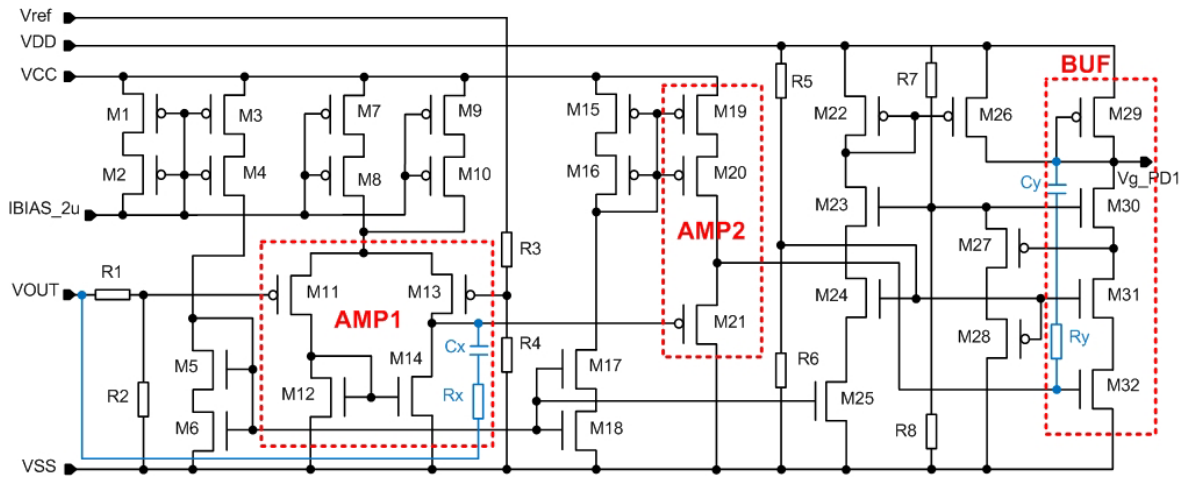


Figure 8. Circuit of the regulator 1.

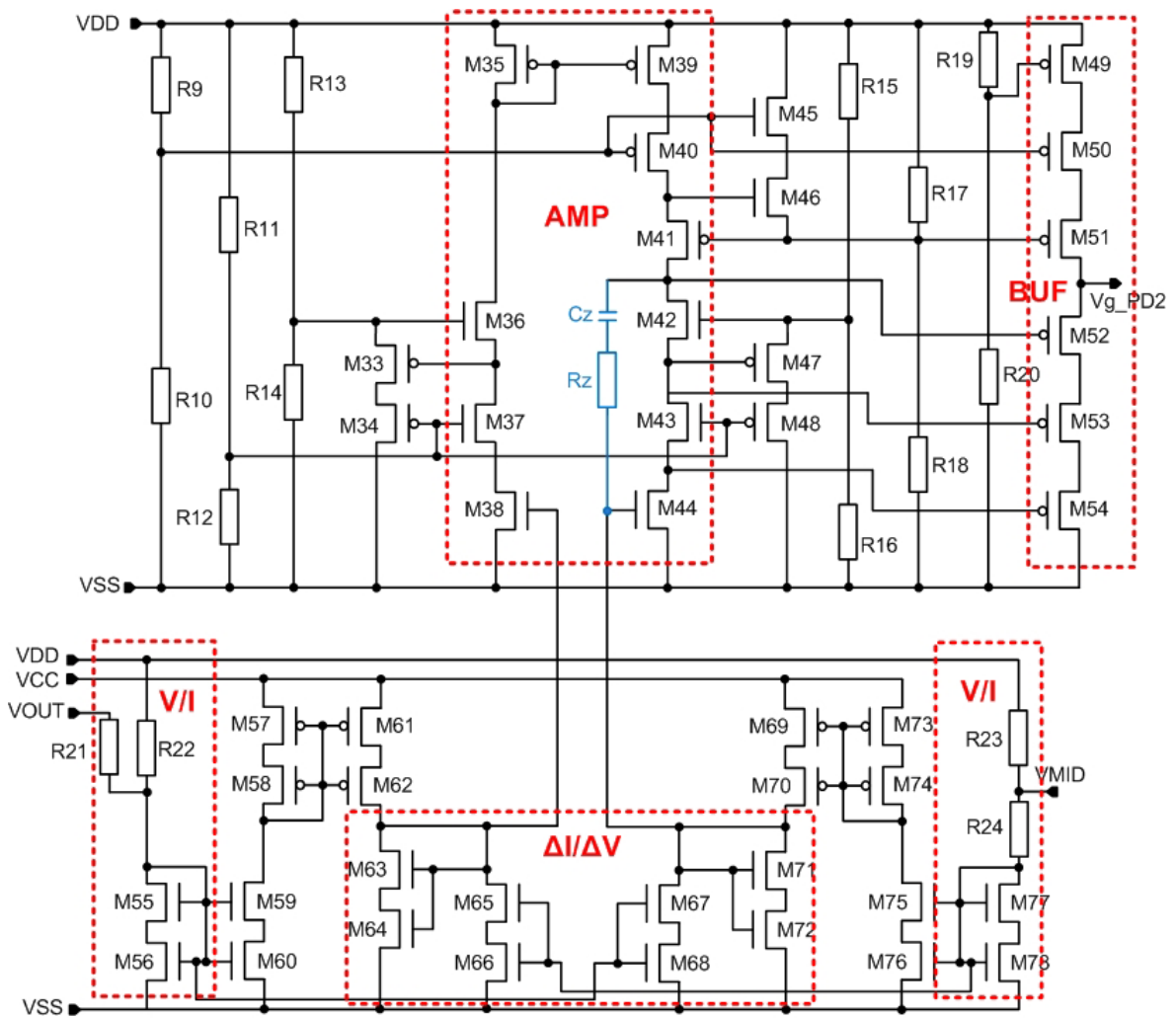


Figure 9. Circuit of the regulator 2.

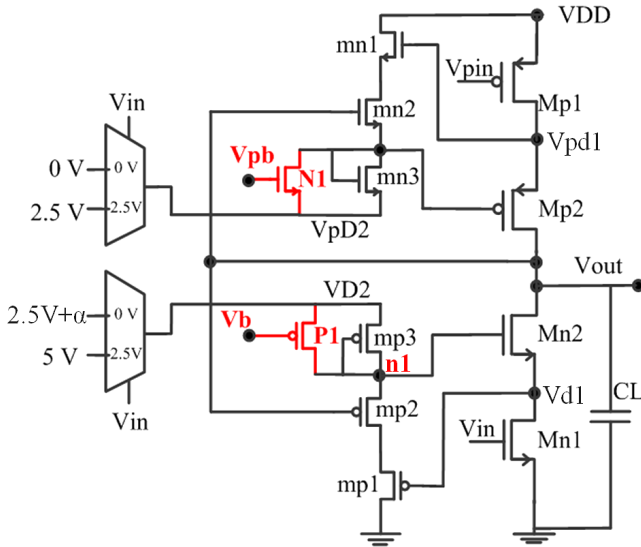


Figure 10. 2-stacked CMOS HV-driver with gate-control circuits.

drain connected and the gate nodes of the other transistors are controlled by the node voltages of the driver V_{d1} , V_{d2} and V_{d3} (drain voltages of the transistors M_{n1} , M_{n2} and M_{n3}).

In on-condition, the voltage of the node 3 ($n3$) can be calculated from the drain current equations of $mp33$, $mp34$ and $mp35$, which are operated in saturation region:

$$\left. \begin{aligned} n2: \quad V_2 &= \frac{V_{D3}}{2} + \frac{V_3}{2} \\ n3: \quad V_3 &= V_{g3} = \frac{V_{d3}}{2} + \frac{V_3}{2} \end{aligned} \right\} \begin{aligned} (3): \quad V_{d3} &= \frac{3 \times V_{out}}{N} \\ \Rightarrow \end{aligned}$$

$$V_{g3} = \frac{2 \times V_{out}}{N} + \frac{V_{D3}}{3}. \quad (12)$$

When the nominal voltage V_n is a fraction of the high-supply voltage V_{HDD} , the supply voltage V_{D3} is switched to 7.5 V in on-condition. The generated voltage V_{g3} (Eq. 12) follows Eq. (2). By connecting 2 pMOS transistors in series (P2 and P3 in Fig. 6), parallel to the gate-drain connected pMOS ($mp34$ and $mp35$), the generated voltage V_{g3} can approach condition of Eq. (7), when V_{HDD} is unequal to $N \times V_n$.

With a similar procedure a circuit generating the gate voltage of the k th stacked nMOS transistor of a high-voltage driver consisting of two groups of pMOS transistors can be described: $k - 1$ gate-drain-connected pMOS and k pMOS transistors must be connected in series. The gate of the k pMOS transistors are controlled by the nodes of the stacked driver. The node between both groups generates the desired gate voltage V_{gk} (Fig. 5c). The supply voltage V_{Dk} switches between $k \times V_n - \Delta V_I$ and $(k - 1) \times V_n$ V according to the on- or off-condition. Current can only flow when the gate-source voltage of each transistor exceeds its threshold voltage, thus limiting the required V_{gk} .

This problem can be solved by connecting pMOS transistors in series biased by reference voltages, in parallel to the gate-drain connected pMOS transistors. When the driver's supply voltage V_{HDD} is not equal to $N \times V_n$, the generated voltage V_{gk} can approach Eq. (6) using these extra pMOSs.

The circuits generating gate voltages of pMOS transistors in the pull-up driver are made up of the complement form of the described circuits. Thus nMOS transistors are used instead of pMOSs (mpk), which are used in the proposed 2-stack CMOS high-voltage driver in 65 nm technology (Fig. 10).

3 Low drop-out voltage regulator (LDO)

3.1 System description

In this work, a low drop-out voltage (LDO) is designed, as can be seen in Fig. 7. It is supplied with 5 V and based on standard low-voltage transistors in 65nm TSMC technology with a nominal voltage of 2.5 V (Dearn et al., 2005; D'Souza et al., 2011; Kuttner et al., 2011). Two-stacked pMOSs (PD1 and PD2) are used as pass transistors. The circuit contains two regulators (Regulators 1 and 2) connected to the gates of pass transistors, respectively. Regulator 1 controls the output voltage (V_{OUT}) according to the reference voltage (V_{ref}) by controlling the first pass transistor PD1. Regulator 2 controls the gate of the second pass transistor (PD2) the partitioning of the high voltage between supply and output between the pass devices PD1 and PD2. In the following sections, the design of both regulators will be described in more detail.

3.2 Regulator 1

Figure 8 shows Regulator 1 composed of a 3-stage amplifier. It is supplied by low voltage V_{CC} of 2.5 V and high voltage V_{DD} of 5 V while comparing the output V_{out} with a reference voltage V_{ref} . The first stage is a single-ended differential amplifier (AMP1) with a pMOS current mirror as active load. Furthermore, the differential amplifier is supplied by the (nominal) low voltage of 2.5 V. To avoid an overvoltage between transistor terminals, both high-voltage input signals (V_{out} and V_{ref}) are reduced to lower voltages by voltage dividers.

The second stage, a common source amplifier (AMP2), is also supplied with a low voltage V_{CC} . It drives the 3rd stage, consisting of a common source amplifier and a MOS diode load operating as a buffer (BUF). It provides both level shifting and low impedance drive to the pass device PD1. This stage utilizes stacked transistors. The first is a main transistor of the CS amplifier, and the 2nd and 3rd transistor shield high voltage. The 4th transistor is a pMOS diode connected to PD1 and controls the drain current of this pass transistor of the LDO.

Table 2. Comparison results between this work (A) and model B.

VDD [V]	Model	t_{LH} [ns]	Δt [ns]	t_{HL} [ns]	Δt [ns]	$R_{n_{on}}\Omega$	$R_{p_{on}}\Omega$
5	B	57		99		687	385
	this work A	42	15	75	24	484	234
	IMPROV.	26.3 %		24 %		30 %	39 %
4.5	B [5]	69.8		90.1		640	471
	this work A	41.2	28.5	71.5	18.6	464	220
	IMPROV.	41 %		21 %		28 %	53 %
4	B [5]	100		82.3		581	680
	this work A	39.6	60.8	66.8	15.5	423	204
	IMPROV.	60.6 %		18.8 %		27.2 %	70 %
3.5	B [5]	220		75		515	1367
	this work A	37.9	182	63.3	11.7	384	195
	IMPROV.	82.7 %		15.6 %		25.4 %	85.7 %

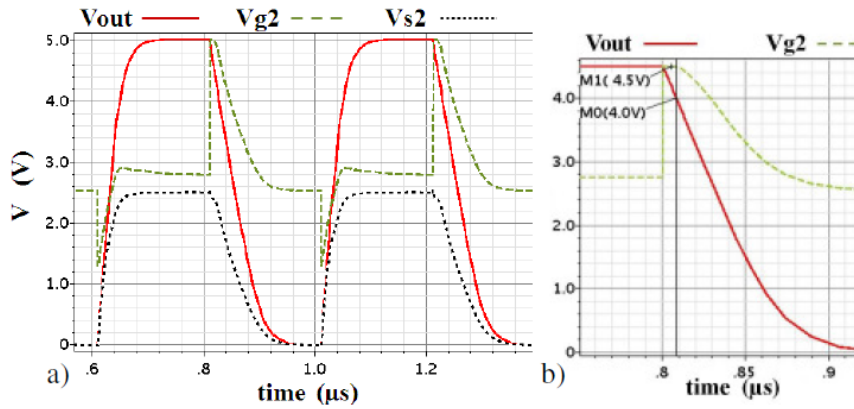


Figure 11. Simulation results of a 2-stacked CMOS driver (a) VHDD = 5 V (b) VHDD = 4.5 V.

Table 3. Transistor dimensions width/length ($\mu\text{m nm}^{-1}$), resistor (Ω) and capacitor (F) values of the Regulator 1.

M1, M2, M3, M4, M7, M8, M9, M10, M15, M16; M19, M20	M5, M6, M17, M18, M22, M23, M24, M25
3/500	1/500
M12, M14, M28	M11, M13, M21
6/500	9/280
M30, M31	M29
4/500	5/500
M32	M26, M27
32/280	2/500
R1, R2, R3, R4, R7	R5, R8
499 K	1.5 M
Rx	Ry
91.2 K	1 M
Cx	Cy
50 p	57 p

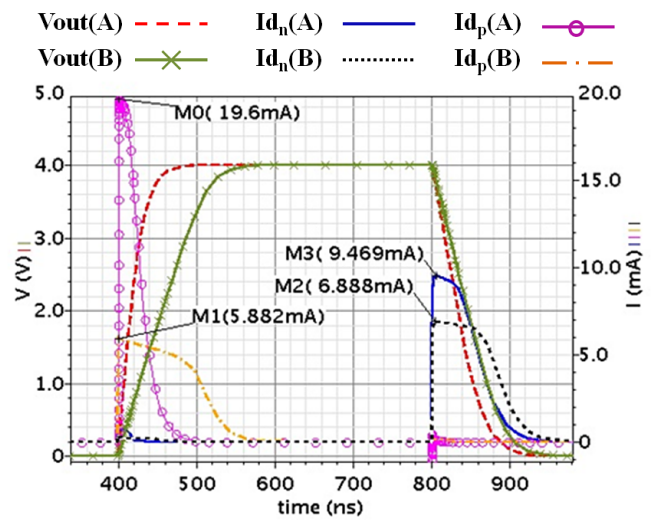


Figure 12. Simulation results of this work in comparison with B.

Table 4. Transistor dimensions width/length ($\mu\text{m nm}^{-1}$), resistor (Ω) and capacitor (F) values of the Regulator 2 and pass transistors.

M35, M39, M38, M44, M55, M56, M65, M66, M67, M68, M77, M78	M33, M46, M47, M57, M58, M61, M62, M63, M64, M69, M70, M71, M72, M73, M74
3/500	2/500
M37, M40, M43	M36, M42, M52
4/500	4/280
M49	M34, M48, M45
5/500	6/500
M50, M51, M53, M4	M41
8/500	8/280
M59, M60, M75, M76	R10, R11, R14, R16, R17, R20
2.4/500	1.5 M
R9, R12	R13, R15, R18
857 K	652.3 K
R19	Rz
326 K	99.59
Cz	PD1, PD2
485.4f	320/280

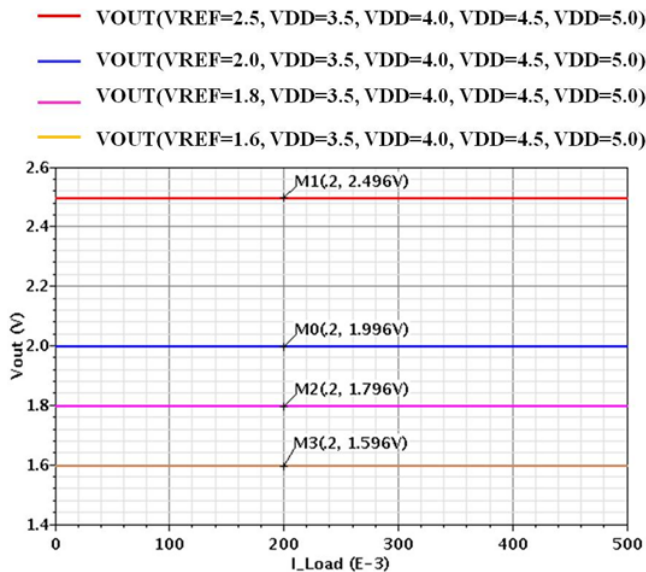


Figure 13. DC simulation of the LDO.

3.3 Regulator 2

Figure 9 shows Regulator 2. This circuit regulates the 2nd-stacked pass transistor PD2 and the actual voltage between PD1 and PD2 (VMID) by comparing this voltage with VMID_REF. VMID_REF is the voltage generated by a voltage divider between the high voltage input VDD and the output VOUT.

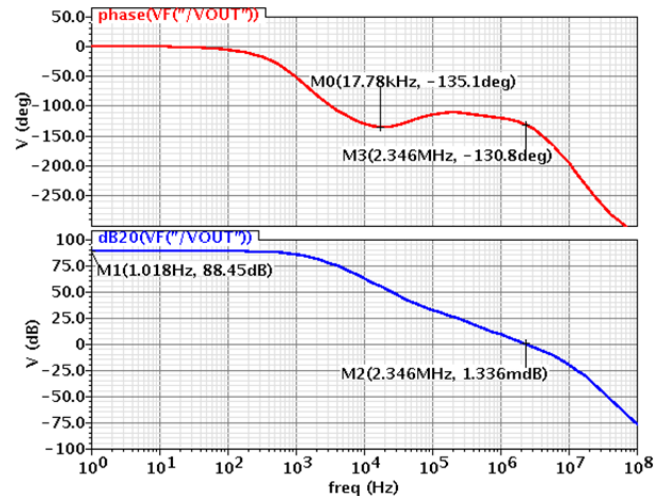


Figure 14. AC characteristics of the open loop (REG1, P1, load).

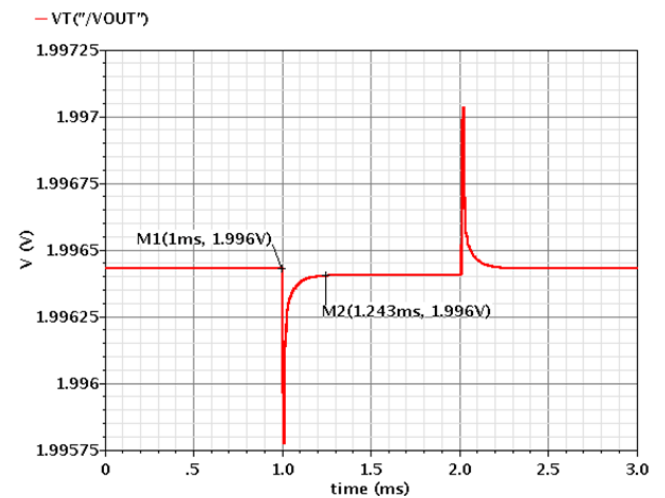


Figure 15. Line regulation (VOUT) with 500 mV input voltage step.

Regulator 2 consists of two parts: a voltage to current converter input with high-to-low voltage level shift function, a differential current to voltage converter and a 3-stage error amplifier. To simplify the design of this high-voltage circuit, the high input voltages VMID and VMID_REF are converted into currents by the voltage to current converter.

The currents are then subtracted from each other in a differential current to voltage converter $\Delta I/\Delta V$, whereas the output voltage is referenced on a MOS diode voltage. This differential voltage controls the pseudo-differential amplifier AMP in the second part. This AMP drives the 2nd stage with nearly rail-to-rail output range. The second stage is intended to operate as a buffer (BUF) and drives the pass transistor PD2 to regulate VMID depending on the difference with VMID_REF.

Transistor dimensions, capacitor and resistor values of the designed circuits are given in Tables 3 and 4.

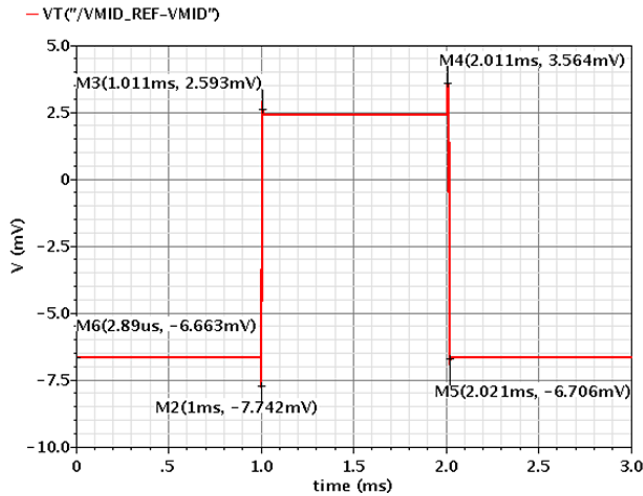


Figure 16. Line regulation (ΔV_{MID}) with 500 mV input voltage step.

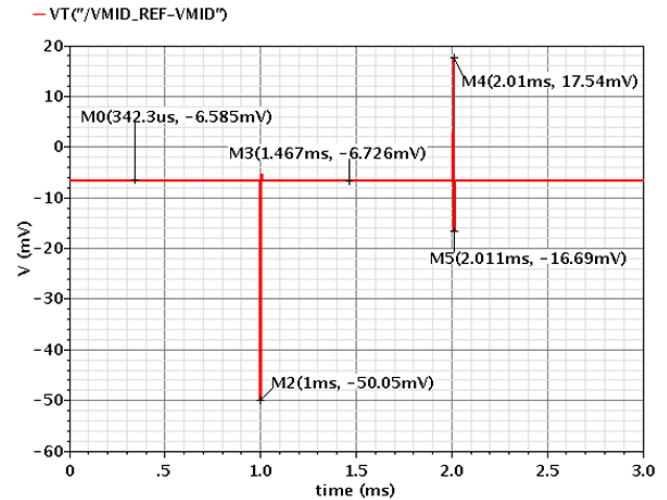


Figure 18. Load regulation (ΔV_{MID}) with 250 mA load current step.

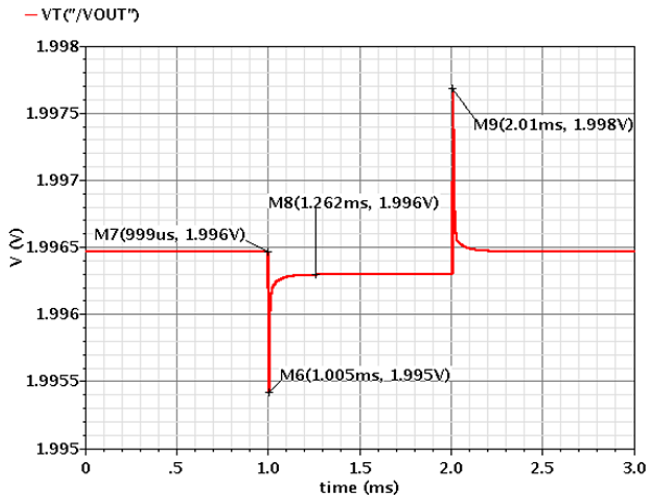


Figure 17. Load regulation (V_{OUT}) with 250 mA load current step.

4 Simulation results

In this section, the simulation results of both proposed high-voltage circuits (the high-voltage driver based on 2-stacked CMOS and the LDO with 2-stacked pass transistors), are presented and described.

4.1 Simulation results of the proposed 2-stacked CMOS high voltage-driver

Figure 10 shows the proposed 2-stack CMOS high-voltage driver in 65 nm technology. V_{in} is the input signal of the pull-down path and V_{pin} , level-shifted from V_{in} , switches the pull-up path. The simulation results of this circuit, supplied with 4.5 and 5 V are shown in Fig. 11a and b, respectively. Figure 11a shows that at logic low input the gate volt-

age V_{g2} switches transistor M_{n2} off by reducing the gate-source voltage below V_{th} . The output voltage V_{OUT} has been charged to 5 V and the source node V_{s2} to 2.5 V, which is half of the output voltage. When the input signal is 2.5 V, the output is discharged from 5 V and V_{s2} from 2.5 to 0 V. The simulation results in Fig. 11a and b show that the voltage V_{g2} follows the rule according to Eqs. (2) and (7) respectively.

Figure 12 shows the output and the drain current of this work (A) in comparison to previous work B (Serneels and Steyaert, 2008) with a supply voltage of 4 V. In the previous work, the gate voltages of the second nMOS and pMOS transistors of a 2-stacked CMOS driver are fixed to the high level of the input signal. The principle of the work B is applied on a 2-stack CMOS driver in 65 nm technology with a nominal voltage of the I/O devices of 2.5 V. The comparison between the results of the rise/fall time and on-resistance of both works with different supply voltages (3.5, 4, 4.5 and 5 V) are given in Table 2. The initial pull-down and pull-up on-resistances of this work are respectively 27–30 and 39–86 % less than B. The rise and fall times of the output voltage of this paper are improved by approximately 24–83 and 16–20 % with a load capacitance of 150 pF. This indicates that the driver is able to switch faster.

The voltage between each transistor's terminals was kept within the nominal technology limit.

4.2 Simulation results of the proposed LDO

Figure 13 shows the simulation results of the proposed LDO output vs. the load current for different values of reference voltages V_{REF} . The output V_{OUT} is maintained constant according to V_{REF} . As the supply voltage drops from 5

to 3.5 V, the output remains constant and follows the reference voltage VREF.

Figure 14 shows the frequency response of the Regulator 1. The AC characteristics are obtained from the open loop gain and phase at the operating point $V_{DD} = 5$ V, $V_{OUT} = 2$ V and a load current $I_{LOAD} = 100$ mA. The frequency of the dominant pole is set with a load capacitance of 4.7 μ F and a load resistance of 20 Ω at 1.69 kHz. The stability of Regulator 1 is achieved by using pole splitting. The second pole, which is set by AMP1, is shifted to a higher frequency at $fp_2 = 371$ kHz with a zero at 41.8 kHz. With compensation, a unity gain bandwidth of 2.7 MHz is achieved. At unity-gain frequency the phase approaches -131° , indicating stability of Regulator 1.

The simulation results of the line regulation response of the proposed LDO are depicted in Figs. 15 and 16. The high-supply voltage VDD is varied from 4.5 to 5 V with rise and fall slew rates of 50 $\text{mV } \mu\text{s}^{-1}$, while the load current remains constant at 100 mA. The steady-state output voltage is $\Delta V_{OUT} = 27$ μ V and the value of the line transient response is about 0.66 mV. The difference between the optimum mid-voltage VMID_REF and VMID is 6.6 mV, and the line regulation response of this difference is 9 mV.

The load regulation response is obtained by the load current ILOAD varied from 5 to 250 mA with rise and fall slew rates of 50 $\text{mA } \mu\text{s}^{-1}$. The simulation results for VOUT and the difference between VMID_REF and VMID are shown in Figs. 17 and 18 respectively.

The load regulation transient response and the steady-state output ΔV_{OUT} are 1 and 0.17 mV respectively. The load regulation of the steady-state of $\Delta(\text{VMID_REF} - \text{VMID})$ is 0.14 mV and its load transient response is 5 and 34 mV respectively for the rising and falling edges of the input signal.

5 Conclusions

In this paper, two high-voltage circuits for power management, a high-voltage driver and an LDO, are presented. The circuits are based on stacked transistors and are compatible with scaled technologies.

For high-voltage drivers, a theory to calculate and design circuits generating gate voltages of stacked transistors to drive a maximum drain current is introduced. By optimally adjusted gate voltages, the driver output provides a minimum on-resistance.

The theory is applied to a 2-stack CMOS driver in 65 nm with a nominal voltage of 2.5 V. Considering the simulation results the gate and source voltages follow the theoretical optimum characteristics. The rise and fall times of the output are improved considerably, which indicate a reduced on-resistance driver. The principle can be applied to N -stack driver transistors as well.

As a second high-voltage circuit for power management, a high-voltage LDO voltage regulator is presented. The circuit is based on the same technology using stacked 2.5 V transistors. An error amplifier controls the main pass transistor and regulates the output voltage. The error amplifier uses 3 stages and has 2 feedback loops, achieving high DC accuracy, as well as good AC and transient characteristics. The second of the stacked pass transistors is controlled by a separate amplifier with lower bandwidth, allowing seamless operation from power down to high load currents. The amplifier equalizes voltage drop across both pass transistors. Therefore, transistor lifetime can be extended and the overvoltage between transistor terminals is avoided. The LDO with stacked devices is suitable for the integration of power management on standard CMOS technologies.

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