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MOS capacitances used in mixed-signal circuits and their operative range

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Abstract. To avoid additional layers for high linearity capacitances in modern CMOS process families, compensated depletion mode MOS capacitances can be used. As shown in previous publications, these MOS capacitances are suitable for low voltage applications.

But there exist limitations concerning the linearity of these capacitances. In this work, the impact of the nonlinearity of the capacitances on different kinds of circuits is investigated. Several examples will be discussed to show how to choose the right capacitance topology.

1 Introduction

In state of the art highly integrated CMOS process families strong design constraints exist concerning the area consumption of a circuit. Often capacitances are the most area intensive components, if you look at mixed-signal circuits, like the sample and hold, the frequency compensation of opamps, or more complex circuits like filters or $\Sigma\Delta$-converters. So it's obvious that it is necessary to search for a method to reduce the area for these capacitances. As shown in Tille et al. (2000) you can use compensated MOS capacitances, because they have a very thin gate oxide, which leads to high area efficiency. Another positive aspect is the knowledge about matching of MOS transistors, because it can easily be transfered to the MOS capacitances. In addition to that no extra process steps are required in contrast to MIM capacitances.

In previous work we have presented $\Sigma\Delta$-modulators using compensated MOS capacitances. The purpose of this work is to investigate the basic analog building blocks of mixed-signal circuits with respect to their sensitivity to the nonlinearity occuring in compensated MOS capacitances. This gives guidelines to the designer for the decision, which type of capacitance is appropriate for a given application.

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2 Device characteristics of MOS capacitances

2.1 C-V characteristic

The usable voltage range of MOS capacitances can be divided in three parts: Accumulation, inversion and depletion. A physical C-V curve of an p-channel MOSFET in an n-well is given in Fig. 1. It shows, that the first two parts behave more linear and have a higher absolute capacitance value than the depletion mode. However, these two voltage ranges are too high for low voltage applications. Concerning the operating point voltages the depletion mode capacitances must be used, but there the value strongly depends on the voltage. The depletion range can be broadened by applying a source bulk voltage (see Fig. 2), but the voltage dependency is still there. In order to reduce this dependency you have to combine two MOS transistors in an antiparallel or antiserial arrangement.

2.2 Compensated MOS capacitances

Most of the nonlinearities of depletion mode MOS capacitances can be eliminated by an antiserial or antiparallel connection of two capacitors (Tille et al., 2000). The exact circuit diagram and the remaining nonlinearity are shown in Fig. 3. Comparing the two methods, you can see that the more area efficient parallel compensation has less linearity than the serial compensation. In both cases you can broaden the usable voltage range by applying an additional source bulk voltage. Just 0.5 V are enough for the serial compensation to get a working range of $\pm$ 1.5 V which is enough for low voltage applications.

The floating source bulk voltages are hard to generate. As the source and drain contacts have to be negative referring to the bulk potential, we can simply connect them to the constant voltage V_{SS}. By doing that we ensure that the drain-bulk and the source-bulk diodes are always reverse-biased. With source and drain on a constant potential and the contacts A and B being variable (see Fig. 4), the depletion broad-

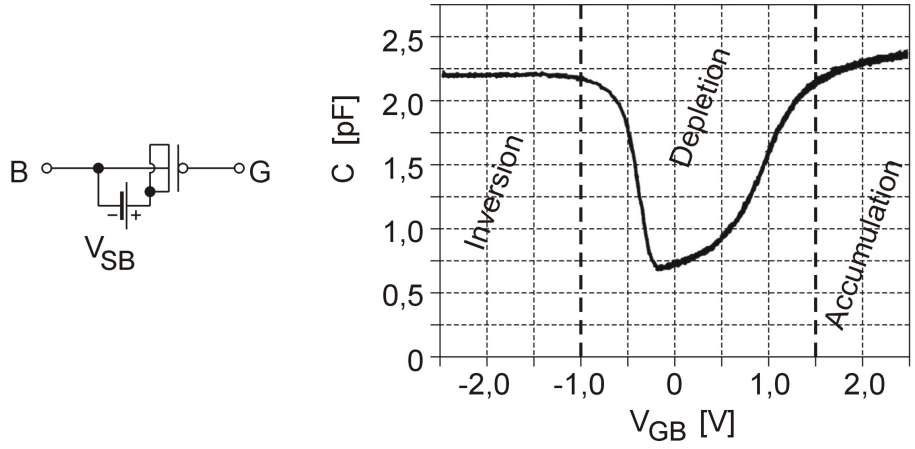

Fig. 1. Measured C-V characteristic of a MOS capacitance and its different voltage ranges.

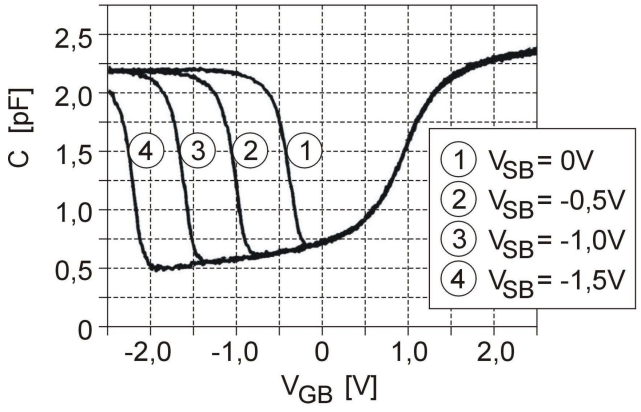

Fig. 2. Measured C-V characteristics of a MOS capacitance with depletion broadening caused by several source bulk voltages.

Table 1. Comparison of the area consumption of different types of capacitances in different technology generations

Process: Type	0.35 μm $[fF/\mu m^2]$	0.25 μm $[fF/\mu m^2]$	0.18 μm $[fF/\mu m^2]$
Poly-Poly	1.30	-	-
Poly-Metal	0.049	0.10	0.10
Metal-Metal	0.041	0.05	0.09
MIM cap.		0.70	0.70
MOS cap. (serial)		0.43	0.49
MOS cap. (parallel)		1.60	1.97

ening is modulated. This does not cause a problem, because in the voltage range $V_{DD} - V_{SS} = 1V$ depletion can be maintained in all operating points, see Fig. 4. With antiserial compensation, the remaining nonlinearity in the voltage range of $[-0.5\,V; 0.5\,V]$ is below 0.5%. For antiparallel compensation we obtain a nonlinearity of nearly 10%, when the full voltage range is used. However, this can be reduced by limiting the voltage amplitude on the capacitance. Within $[-0.3\,V; 0.3\,V]$, the nonlinearity is only around 3%.

To complete the introduction of compensated depletion mode MOS capacitances, Table 1 gives a comparison of the area consumption of different types of capacitances in different technology generations. Here it has to be kept in mind, that MIM capacitances have a big drawback. They need additional process steps, which leads to higher process complexity.

3 Analog circuit blocks with compensated depletion mode MOS capacitances

To demonstrate the usability of MOS capacitances, four different analog circuit blocks have been simulated, representing the basic components of mixed-signal circuitry. To determine which circuits are sensitive to nonlinearity, the parallel compensation was assumed as worst case. This shows the impact of area efficiency on the linearity of mixed-signal circuits.

3.1 Sample and hold

In the sampling mode, the capacitance is charged up to the input voltage. With a nonlinear capacitance, the amount of charge is nonlinearly dependent on the input voltage. In the hold mode, the sampled voltage is evaluated by connecting it to a high-ohmic node, most often to the input of an operational amplifier. Therefore the nonlinearity of the $C(V)$ and $Q(V)$ characteristics do not influence the circuit function. To check this in a complete system, we exchanged the sampling capacitance in a sample and hold circuit between an anti-aliasing filter and an A/D-converter and replaced it with an antiparallel compensated MOS capacitance. The simulations showed no decrease of SNDR, confirming that there is no degradation of linearity.

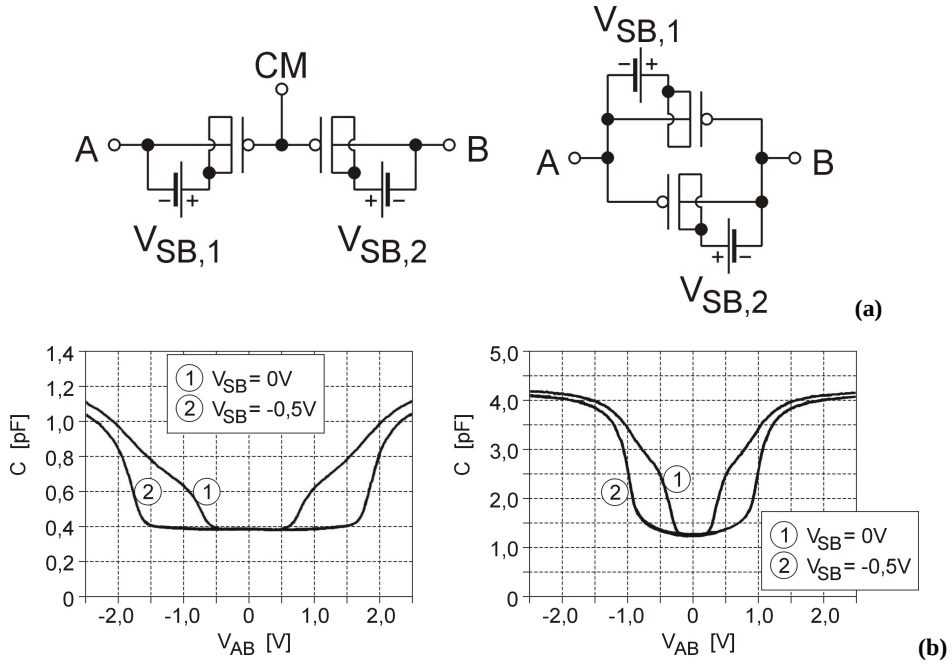

Fig. 3. Circuit diagram and measured C-V characteristics of an antiserial (left) and an antiparallel (right) compensated depletion mode MOS capacitance.

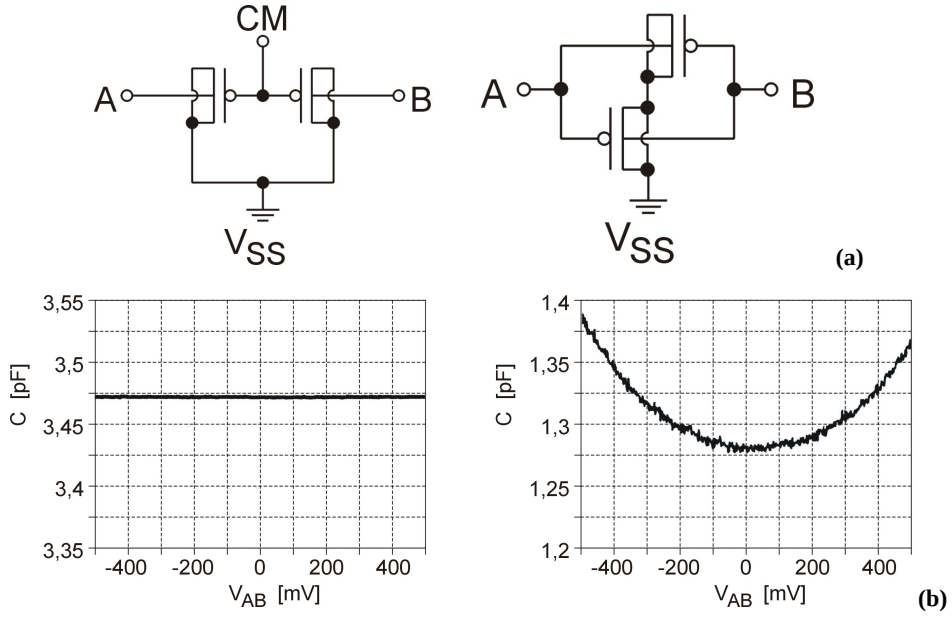

Fig. 4. Circuit diagram and measured C-V characteristics of an antiserial (left) and an antiparallel (right) compensated depletion mode MOS capacitance without floating sources.

3.2 Frequency compensation of operational amplifiers

The design constraint for the frequency compensation of opamps is stability. As an example we discuss the lead lag compensation method using parallel compensated MOS capacitances as shown in Fig. 5.

The lead lag network adds a pole and a zero to the transfer function of the opamp. In this example the pole is at about 10 kHz and the zero at about 100 kHz. Both of them depend on the compensated capacitance. A problem arises, if the pole/zero-shift, caused by the nonlinearity of the capacitance, influenced the phase margin. But Fig. 5 also shows that a small shift would have only little effect on the 0 dB limit and the phase will only change in part 1 of the frequency range. The 0 dB frequency is placed in part 2, so the pole/zero-shift will have no effect on the stability. That's

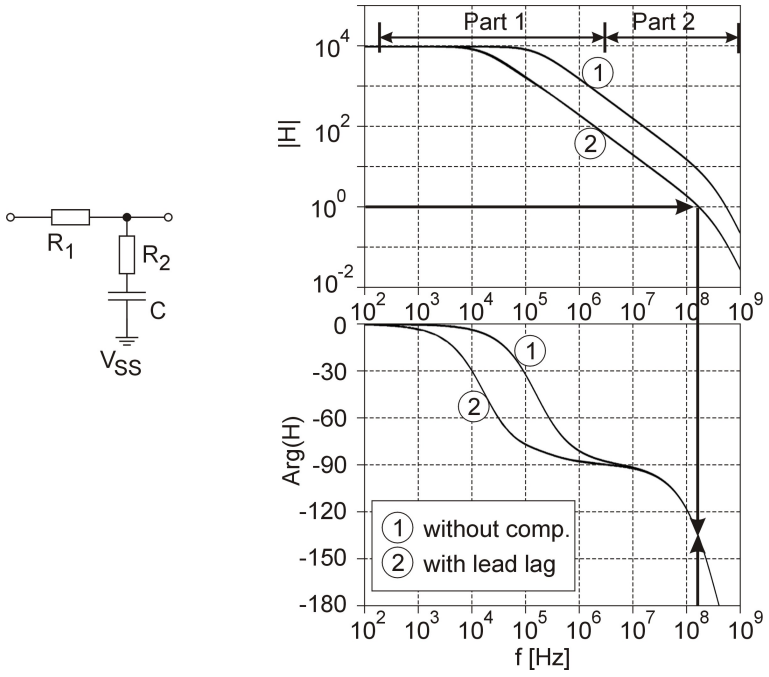

Fig. 5. RC-network and bode diagram of the lead lag frequency compensation method for operational amplifiers.

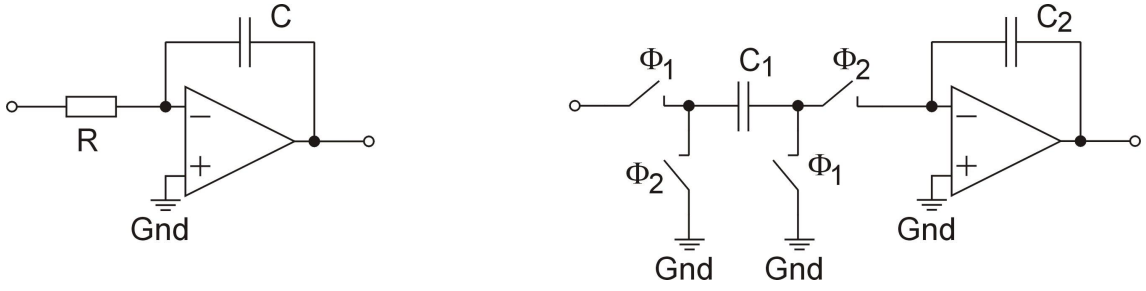

Fig. 6. A simple RC integrator on the left and a SC integrator on the right side.

why we can use the most area efficient method, the parallel compensation (Sauerbrey et al., 2002).

3.3 Switched capacitor low pass filter

For this investigation a second order switched capacitor filter with a bandwidth of $f_g = 100\,\text{kHz}$ and a sampling frequency of $f_S = 5\,\text{MHz}$ has been used, where all linear capacitances were replaced by parallel compensated MOS capacitances. The usability has again been evaluated with the help of the signal to noise and distortion ratio.

In Table 2, the signal to noise and distortion ratios for different input amplitudes are given. The SNDR decreases for increasing input amplitude. This can be explained regarding the operation mode of the filter in the two clock phases of the SC system. In the first phase, the input capacitance C_1 is charged with $Q_{C1}(V_{in})$, where a certain nonlinearity is presented in the function $Q(V)$. This charge is transferred to the output capacitance C_2, giving rise to an output voltage determined by $Q_{C2}(V_{out}) = Q_{C1}(V_{in})$. As C_1 and C_2 usually are not equal, their nonlinearities will not cancel. This leads to harmonics in the output signal and therefore reduce the SNDR. This effect increases with the amplitude, as can be seen from Fig. 4. The example of Table 2 represents the worst case, as only parallel compensated capacitances were used. This is sufficient for a SNDR of 60 dB or a resolution of about 10 bit. A much higher accuracy can be obtained by using serial instead of parallel compensated MOS capacitances. In this way the area consumption can be optimized concerning the needed accuracy.

3.4 Integrators

The analysis of the RC integrator (Fig. 6) is relatively easy. You just have to realize that the inverting input of the opamp is at virtual ground. So the C-V dependency of the integration capacitance appears directly at the output of the integrator.

Concerning the SC integrators $C_2(V_{out})$, the same dependency exists as in the RC integrator. In addition to that, there

Table 2. Simulated SNDR of a second order SC low pass filter with a bandwidth of $f_g = 100\,\text{kHz}$ and a sampling frequency of $f_S = 5\,\text{MHz}$, realized with parallel compensated depletion mode capacitances

Input Amplitude	Signal to Noise and Distortion Ratio [dB]
50 mV	84.6
100 mV	71.4
200 mV	60.9

is a voltage dependent deviation caused by the input capacitance $C_1(V_{in})$. So with very small input amplitudes the SC-Integrator will be as good as the RC integrator, but it gets worse with increasing input amplitudes.

For the integrators we can also summarize, that the area efficiency strongly depends on the needed accuracy for the individual application.

4 Conclusion

The mixed-signal circuit designer has not only to consider the functionality of a circuit, but also the amount of resources needed. In some circuit blocks there is no problem using the highly area efficient parallel compensated depletion mode MOS capacitances, like in the sample and hold or the frequency compensation of opamps. In other blocks the appropriate capacitance topology dependent on the specifications of the application has to be chosen. A combination can be suitable in complex mixed-signal circuits like $\Sigma\Delta$-modulators. They are quite insensitive to parameter variations due to their special feedback structure. So you just have to spend serial compensated MOS capacitances at a few key instances, where particularly high linearity is needed. All other capacitances can be realized by area efficient parallel compensated MOS capacitances.

This work shows, that compensated depletion mode MOS capacitances are suitable for low voltage applications in future technology generations.

References

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